Circuit Design

D1.4

1000BASE-T Integrated Network Interface & Current-Mode PHY

Non-PoE | TD magnetics | Current-mode architecture with external termination

Design Overview

1. PHY-Side Termination and Bias

R1-R8 are 49.9Ω ±1%. Each of the eight MDI lines connects to VBIAS through its own resistor. All four PHY-side center taps, CT_A-CT_D, also connect to VBIAS.

2. Local Bypass at Every Location

Place C1-C4 near the termination of each pair and C5-C8 near the four CTs. Each 10nF capacitor bypasses VBIAS to GND. Retain local bypass at each location even though the supply net is shared.

3. TD Structure and Four Data Pairs

Each channel comprises a 1:1 isolation transformer and a CMC. Pairs A/B/C/D connect to RJ45 contacts 1/2, 3/6, 4/5 and 7/8, respectively. All four pairs transmit and receive bidirectionally.

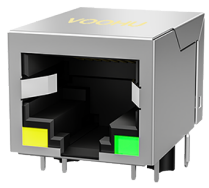
4. Common-Mode Termination and Shield

Each cable-side transformer CT connects through 75Ω to BS, then through CBS (1nF / HV) to SHIELD. The metal shell connects directly to SHIELD. The illustrated Bob Smith network is internal to J1.

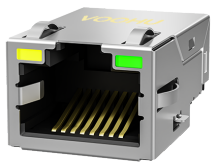
5. Scope

Non-PoE; current-mode architecture requiring external termination and CT bias power. Verify VBIAS, final bypass values and module specifications for the selected parts. No GND-to-SHIELD coupling network is shown.

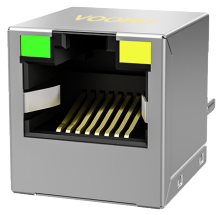
Product Illustrations



- SYT-320DNL



- SYT211Q106-DB1A7CBS057

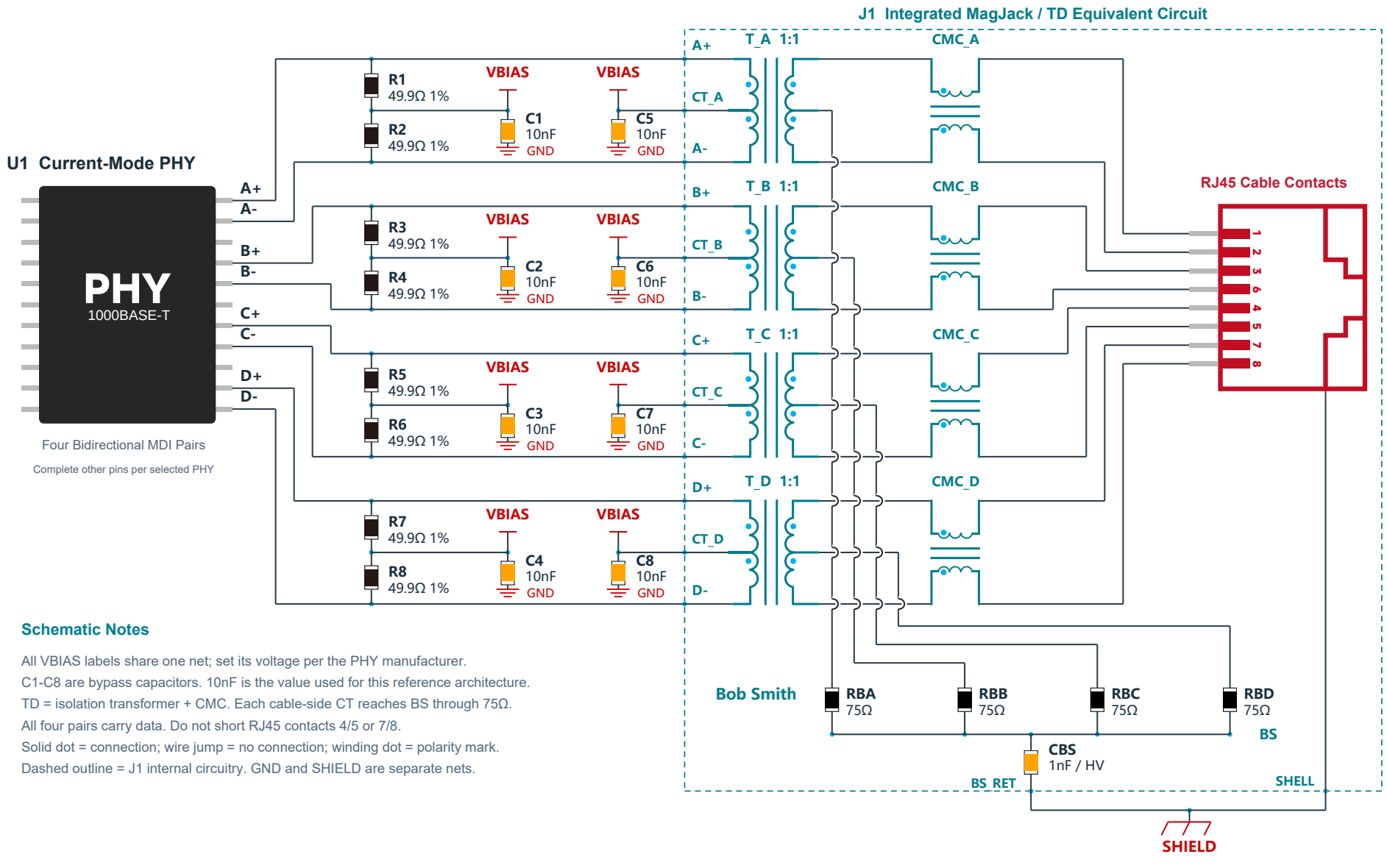


- SYT511Q070-AB1A8D



- SYT21Q042-DB2A4D068

Reference Schematic

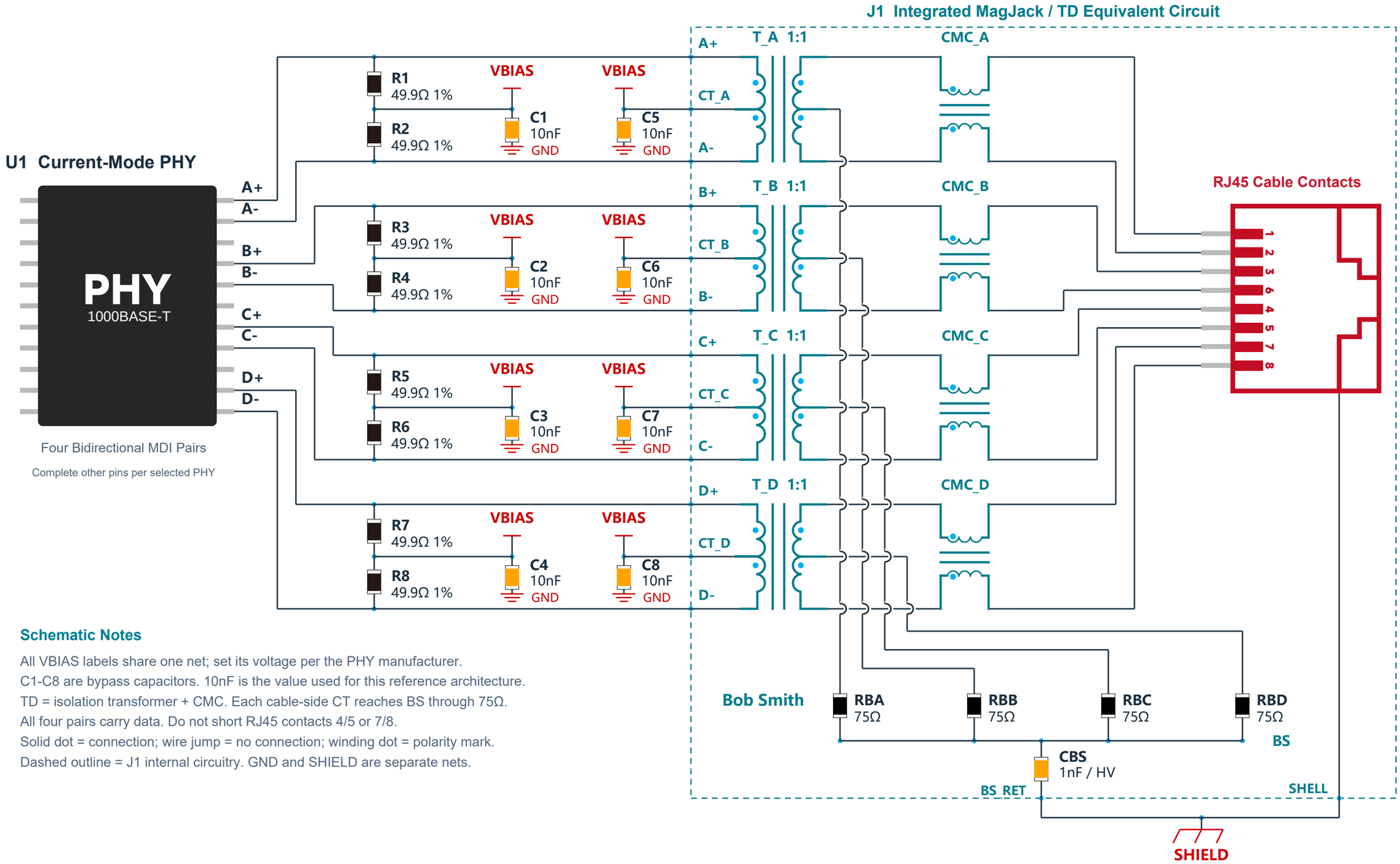


Schematic Notes

All VBIAS labels share one net; set its voltage per the PHY manufacturer.
C1-C8 are bypass capacitors. 10nF is the value used for this reference architecture.
TD = isolation transformer + CMC. Each cable-side CT reaches BS through 75Ω.
All four pairs carry data. Do not short RJ45 contacts 4/5 or 7/8.
Solid dot = connection; wire jump = no connection; winding dot = polarity mark.
Dashed outline = J1 internal circuitry. GND and SHIELD are separate nets.

1000BASE-T Integrated Network Interface & Current-Mode PHY

Non-PoE | TD magnetics | MDI analog interface only



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Component Functions and Connections

Electrical design is based on semiconductor manufacturers' documentation. The old artwork supplies symbols and product illustrations only. Functional names and values do not specify purchasing part numbers.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / Current-Mode PHY	1, outside J1	All four MDI pairs are bidirectional. This circuit is limited to an architecture requiring external shunt termination and powered PHY-side CTs. Complete the other power, clock, reset and MAC connections for the selected PHY.	TI E1 §8; Microchip E2 pp.2-4
R1-R8 / 49.9Ω ±1%	8, outside J1	Pair A uses R1/R2; B uses R3/R4; C uses R5/R6; D uses R7/R8. Each line connects to VBIAS through its own resistor to provide termination and bias. Do not connect the termination midpoint to GND.	TI E1 p.10, Fig.8; Microchip E2 pp.2-3
C1-C4 / 10nF	4, outside J1	Bypass the termination midpoints of A/B/C/D locally from VBIAS to GND, reducing the high-frequency impedance of the bias network at each termination. 10nF is taken from the reference architecture; it is not a universal requirement for every PHY.	TI E1 p.10
C5-C8 / 10nF	4, outside J1	Locally bypass CT_A/CT_B/CT_C/CT_D, respectively. Each CT connects directly to VBIAS; its capacitor forms a shunt branch to GND. Do not assume a single capacitor can replace local bypasses simply because they share a named supply net.	TI E1 p.10, Fig.8
VBIAS / Bias Net	Same-name nodes are connected	Provides the required bias for eight termination resistors and four PHY-side CTs. Confirm the voltage and permitted maximum with the PHY specification. This schematic does not fix VBIAS at 3.3V or treat it as circuit ground.	TI E1 p.10; Microchip E2 pp.2,4
T_A-T_D / 1:1	4 channels, inside J1	Transfer differential signals and isolate the PHY from the cable. PHY-side CTs connect to VBIAS; cable-side CTs connect to their respective 75Ω resistors. The turns ratio is 1:1; inductance, loss, crosstalk and isolation conditions must match the PHY.	Microchip E2 pp.3-4; E4 p.5, Fig.3
CMC_A-CMC_D	4 channels, inside J1	Two-winding common-mode chokes are in series with both cable-side data lines. Together with the isolation transformers they form TD channels and suppress common-mode interference. Differential insertion loss and frequency response must also meet signal requirements.	Microchip E4 pp.4-5, Fig.3
TD / Four Channels	4 × T + 4 × CMC	TD here means an isolation transformer plus a common-mode choke, without an autotransformer winding. Bob Smith termination is taken from the transformer cable-side CT before the CMC. PHY-side CTs remain isolated from these nodes.	Microchip E4 p.5, Fig.3; Microchip E2 p.4
RBA-RBD / 75Ω	4, inside J1	Each cable-side CT of T_A/T_B/T_C/T_D connects to the common BS node through its own 75Ω resistor. Join the branches only after the resistors; do not short the four CTs together first. Do not add duplicate resistors externally.	Microchip E2 p.4; E4 p.5, Fig.3
CBS / 1nF, HV	1, inside J1	AC-couples BS to SHIELD and blocks DC in this branch. 1nF appears in E1/E2; E1 shows 3kV and E2 shows 2kV. Confirm the final voltage rating and test conditions for the selected module. CBS is not a surge clamp.	TI E1 p.11; Microchip E2 p.4
J1 / RJ45 and Shield	1 integrated module	Map A to 1/2, B to 3/6, C to 4/5 and D to 7/8; all are data pairs. SHELL connects directly to SHIELD. The dashed outline defines module ownership. The illustrated module includes four TD channels, 75Ω resistors and CBS; verify each feature during selection.	Microchip E2 pp.4-5; Microchip E4 §3.8
GND / SHIELD	Two separate nets	GND is the PHY circuit ground. The shield side of CBS and the metal shell share SHIELD. The schematic does not define the system-level relationship between GND, chassis and PE, and contains no additional RC coupling branch.	TI E1 p.11; Microchip E2 p.5

Technical Sources and Scope of Use

E1 · Texas Instruments — AN-1263 / SNLA056D, Rev.D, 2013, pp.10-11. Used only for external termination, CT bias and local bypass. The TDA drawing on p.14 is not the basis for the TD structure used here.

E2 · Microchip / SMSC — LAN8810 QFN Schematic Checklist, Rev.B, 2014, pp.2-5. Used to cross-check termination, CT supply, pair mapping, Bob Smith termination and shielding.

E3 · Motorcomm — YT8511 Application Notes, V1.2, p.3; public reproduction of manufacturer-attributed material. It describes voltage-mode output with on-chip termination and is used only to exclude that architecture, not to justify this current-mode connection.

E4 · Microchip / Microsemi — ENT-AN0098 / VPPD-01740, Rev.2.2, June 2018, printed pp.4-5 (PDF pp.6-7), Fig.3. Used only for the TD structure with cable-side two-winding CMC and CT termination location. PHY-side CT supply still follows E1/E2.

Scope: a non-PoE MDI interface reference. After selecting the PHY and MagJack, recheck parameters, package pin mapping and system grounding, then validate link, MDI, EMC and insulation performance. Review of this document does not replace hardware testing.