Circuit Design

1000BASE-T Surge and ESD Protection & Current-Mode PHY

Design Overview

1. Scope

Non-PoE, four bidirectional 1000BASE-T pairs; discrete RJ45 with external TD magnetics and reliable chassis/PE. For current-mode PHYs requiring external split termination, capacitively grounded termination midpoints and biased CTs.

2. Termination and Bias

R1-R8 are 49.9Ω each. Each pair's midpoint connects to GND through its own 10nF capacitor, without a direct connection to supply or GND. PHY-side CTs connect to VCT; the voltage follows the selected PHY. C5-C8 (100nF each) are local bypass recommendations for this design.

3. Magnetics and Contacts

T1 contains four 1:1 isolation transformers with cable-side CMCs. Pairs A/B/C/D connect to RJ45 contacts 1/2, 3/6, 4/5 and 7/8. All four pairs carry data; do not short contacts 4/5 or 7/8.

4. Staged Protection

D1-D4 are low-capacitance bidirectional TVS devices on the PHY side, each across one differential pair. G1-G4 connect the cable-side CTs to SHIELD, before the 75Ω resistors. Connect SHIELD to reliable chassis/PE.

5. Common-Mode Termination and Implementation

Each cable-side CT connects through RB1-RB4 (75Ω each) to BS, then through C9 (1nF, ≥2kV) to SHIELD. The metal shell shares SHIELD; GND remains separate. Select protection parts for the actual PHY and test conditions. See page 3 for parameters and sources.

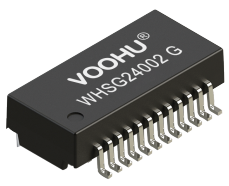
Product Illustrations



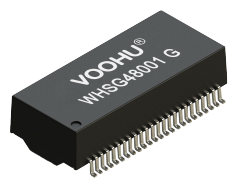
- SYT561188-AB1A3DY1027



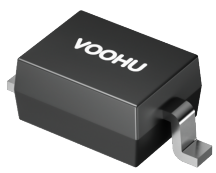
- SYT60S1188-AB1A6DY1008



- WHSG24002G



- WHSG48001G

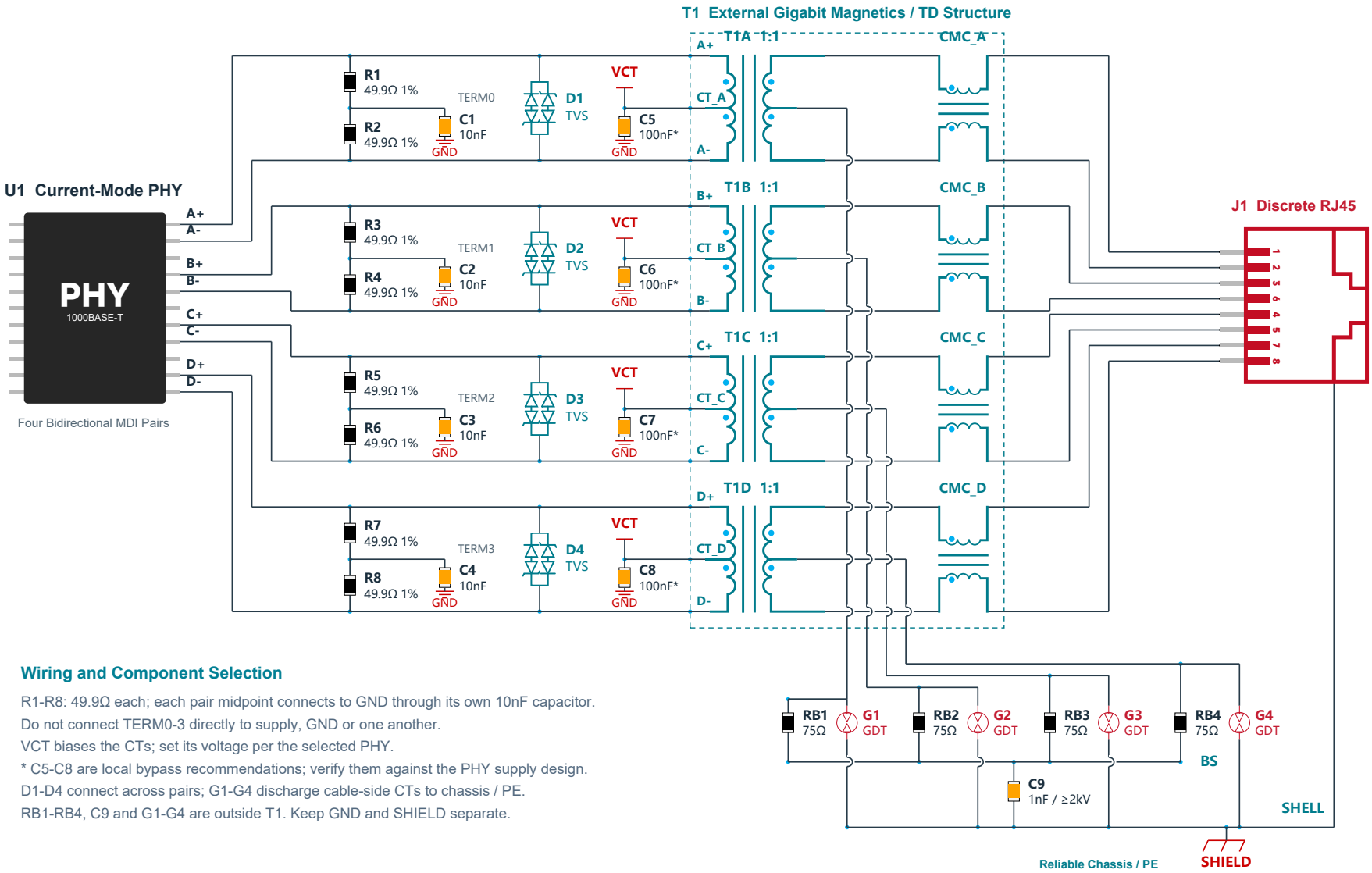


- WHTA3V30P8B



- WHGD090V1P0B

Reference Schematic



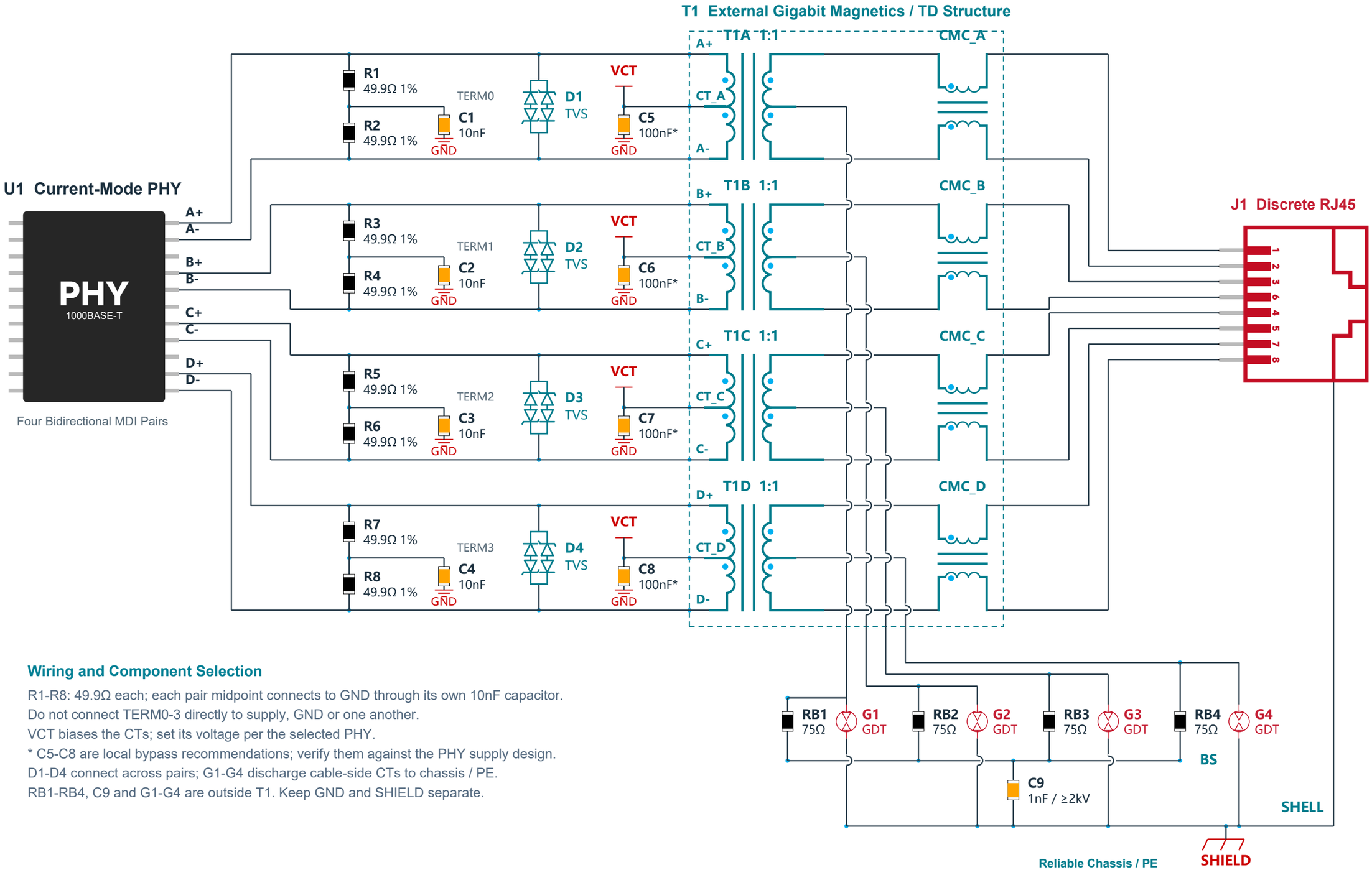
Wiring and Component Selection

R1-R8: 49.9Ω each; each pair midpoint connects to GND through its own 10nF capacitor.
Do not connect TERM0-3 directly to supply, GND or one another.
VCT biases the CTs; set its voltage per the selected PHY.
* C5-C8 are local bypass recommendations; verify them against the PHY supply design.
D1-D4 connect across pairs; G1-G4 discharge cable-side CTs to chassis / PE.
RB1-RB4, C9 and G1-G4 are outside T1. Keep GND and SHIELD separate.

Reference circuit for design and component selection. Final connections, component parameters and protection performance depend on actual selection and system validation.

1000BASE-T Surge and ESD Protection & Current-Mode PHY

1000BASE-T | Non-PoE | External split termination / CT bias | Reliable chassis / PE



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Functional names are not package pins; RJ45 numbers are cable contacts. Solid dot = connection; winding dot = polarity mark; wire jump = no connection. Protection selection: page 3.

Component Functions, Sources and Validation Conditions

The termination follows a Gigabit current-mode example and is combined with GDTs and differential TVS protection. Each stage has public manufacturer evidence; the combined design has not been system-tested and has no confirmed kV protection level.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / R1-R8 / C1-C4	1 PHY; 8 resistors; 4 capacitors	Applicable only to the illustrated termination architecture. Each pair uses 2 × 49.9Ω (±1%) with its midpoint connected to GND through 10nF. Do not directly join the four midpoints or connect them directly to VCT or GND. Independent midpoints reduce common-mode coupling; differential termination is approximately 100Ω.	E1 sheet 7; resistor tolerance: engineering recommendation
VCT / C5-C8	4 × 100nF*, outside T1	The four PHY-side CTs connect to a bias supply. The 88E1111 example uses 2.5V; this cannot be transferred directly to other PHYs. *100nF close to each CT is a local bypass recommendation for this design. Verify capacitance, quantity and supply filtering against the selected PHY and PCB power design.	VCT: E1, E2; bypass configuration: engineering recommendation
T1A-T1D / CMC	4 channels, inside T1	Each TD channel is a 1:1 isolation transformer plus cable-side CMC. Preserve winding dots and polarity. Magnetics must meet the selected PHY requirements for insertion loss, return loss, inductance, balance and insulation. Also verify the winding and CMC pulse withstand capability in the CT surge path.	Structure: E3 Fig.7; parameters: PHY and magnetics manufacturers
D1-D4 / Bidirectional TVS	4 differential protection channels	Connect across P/N of each pair on the PHY side, close to the magnetics. Choose low-capacitance parts suitable for Gigabit signals. VRWM must cover the normal differential swing; clamping and energy at the actual surge current must match the PHY transient limits. No single voltage rating applies universally.	E4 Fig.4; parts and parameters pending selection
G1-G4 / GDT	4 branches, outside T1	Each cable-side CT connects through a GDT to SHIELD/PE before its 75Ω resistor. Coordinate sparkover voltage, impulse current, residual voltage and firing differences with the magnetics, TVS and port insulation test. Do not choose 90V solely because it appeared in an old drawing.	Local connection: E5 p.8; non-PoE combination: engineering design
RB1-RB4 / 75Ω	4, outside T1	Each cable-side CT passes through 75Ω before joining BS for common-mode termination. These resistors do not replace GDTs or TVS devices. Calculate pulse power before GDT firing and under residual surge stress. ±1% is an engineering selection recommendation.	Connection/value: E3 p.11; pulse check: engineering requirement
C9 / 1nF, ≥2kV	1, outside T1	The high-voltage capacitor connects BS to SHIELD for a high-frequency common-mode return. ≥2kV is a reference component-rating recommendation. Verify the actual AC/DC ratings, insulation and residual surge stress. It does not establish a 2kV or higher system surge rating.	E3 p.11; final insulation coordination to be verified
J1 / GND / SHIELD	Discrete RJ45; separate nets	A/B/C/D map to 1/2, 3/6, 4/5 and 7/8. SHELL, GDTs and C9 return to reliable chassis/PE. GND stays on the PHY side; no fixed GND-SHIELD coupling branch is shown. Complete actual pin mapping, LEDs and all PHY peripherals for the selected parts.	E3; reliable chassis/PE confirmed by user; mapping per this schematic

Manufacturer Sources and Scope of Use (click to open)

E1 · Altera
Cyclone IV GX development board, 150-0311002-B1 Rev.B, March 3, 2010, sheet 7 of 15. The 88E1111 uses two 49.9Ω resistors per pair and an independent 0.01µF midpoint capacitor to GND. Only the Gigabit termination example is adopted, not the board's complete grounding design.

E2 · Marvell
88E1111 Datasheet, MV-S100649-00 Rev.M, August 31, 2020, p.190, §4.4.3 and Table 125: the external magnetics CT supply is 2.5V. This value applies only to the 88E1111; the generic schematic retains VCT for the selected PHY to define.

E3 · Texas Instruments
TIDA-00204 Design Guide, TIDU832B, July 2017, p.11, §2.3.1.1.3 and Fig.7. Four cable-side CTs each pass through 75Ω and a shared 1000pF capacitor to chassis; the recommended capacitor rating is ≥2kV. Only the cable-side network is adopted, not its voltage-mode PHY termination or test levels.

E4 · Semtech
Ethernet Protection Methodology, February 19, 2020, Fig.4 and conclusions. TVS devices connect across pairs on the PHY side. Selection follows the PHY damage threshold and surge current. This does not establish the protection level of this design.

E5 · Littelfuse
General Port Protection, 2024, p.8. The original is a PoE++ example. Only the local topology of four cable-side CTs discharging through GDTs to ground is used. Its non-PoE adaptation and combination with E1/E4 are engineering design decisions without system-level validation.

PCB Implementation and Protection Validation

Use 100Ω differential MDI routing. Place termination close to the PHY and TVS devices close to the magnetics; keep branches short and symmetric. Make GDT-to-PE paths short and wide, separated from PHY-side routing and reference planes. Define ESD/surge levels, waveforms, coupling, source impedance and acceptance criteria before validating the link, signal integrity, residual voltage, component pulse stress and insulation. This design does not cover PoE, direct lightning strikes or sustained power-frequency faults. Displayed products have not been confirmed as compatible.

Schematic text and connection data have been checked. No native EDA ERC, prototype protection testing or system certification has been performed.