Circuit Design

D1.0

1000BASE-T Network Interface & Gigabit Magnetics & Voltage-Mode PHY

Non-PoE | Discrete RJ45 + external magnetics | Voltage-mode PHY with on-chip termination

Design Overview

1. PHY-Side Interface

All four MDI pairs transmit and receive bidirectionally. Use a voltage-mode PHY with on-chip termination. Do not add duplicate 49.9Ω termination on the data lines or an external bias supply to the PHY-side center taps (CTs).

2. Four Independent Center Taps

Connect CT_A-CT_D individually to GND through C1-C4 (100nF each), with each capacitor close to its magnetics pin. Do not short the four CTs together or connect them directly to GND.

3. Gigabit Magnetics and Pair Mapping

T1 contains four 1:1 isolation transformers with common-mode chokes (CMCs), forming a TD structure. Pairs A/B/C/D connect to RJ45 contacts 1/2, 3/6, 4/5 and 7/8, respectively. All four are data pairs.

4. Common-Mode Termination and Shield

Each cable-side CT connects through R1-R4 (75Ω each) to BS, then through C5 (1nF / 2kV) to SHIELD. These resistors and capacitor are external PCB components. Connect the RJ45 metal shell to the same SHIELD.

5. Scope

Non-PoE; for PHYs with on-chip termination and capacitively grounded CTs. Keep GND and SHIELD as separate nets; define their relationship at system level. Complete the power, clock, reset and MAC interface for the selected PHY.

Product Illustrations



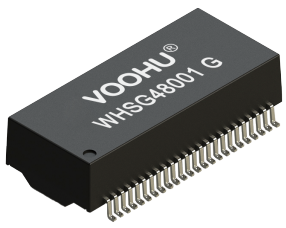
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- SYT60S1188-AB1A6DY1008

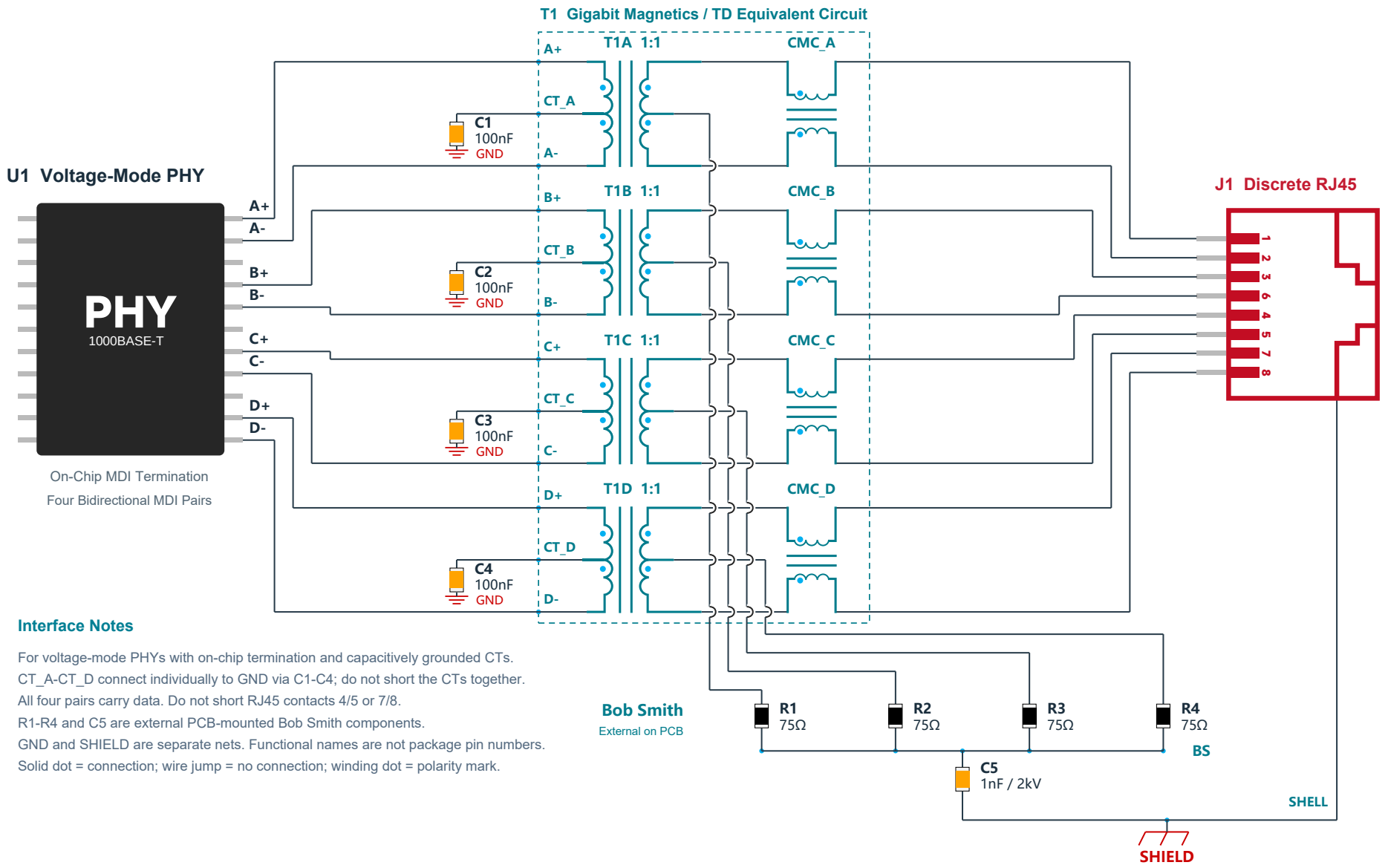


- WHSG24002G



- WHSG48001G

Reference Schematic

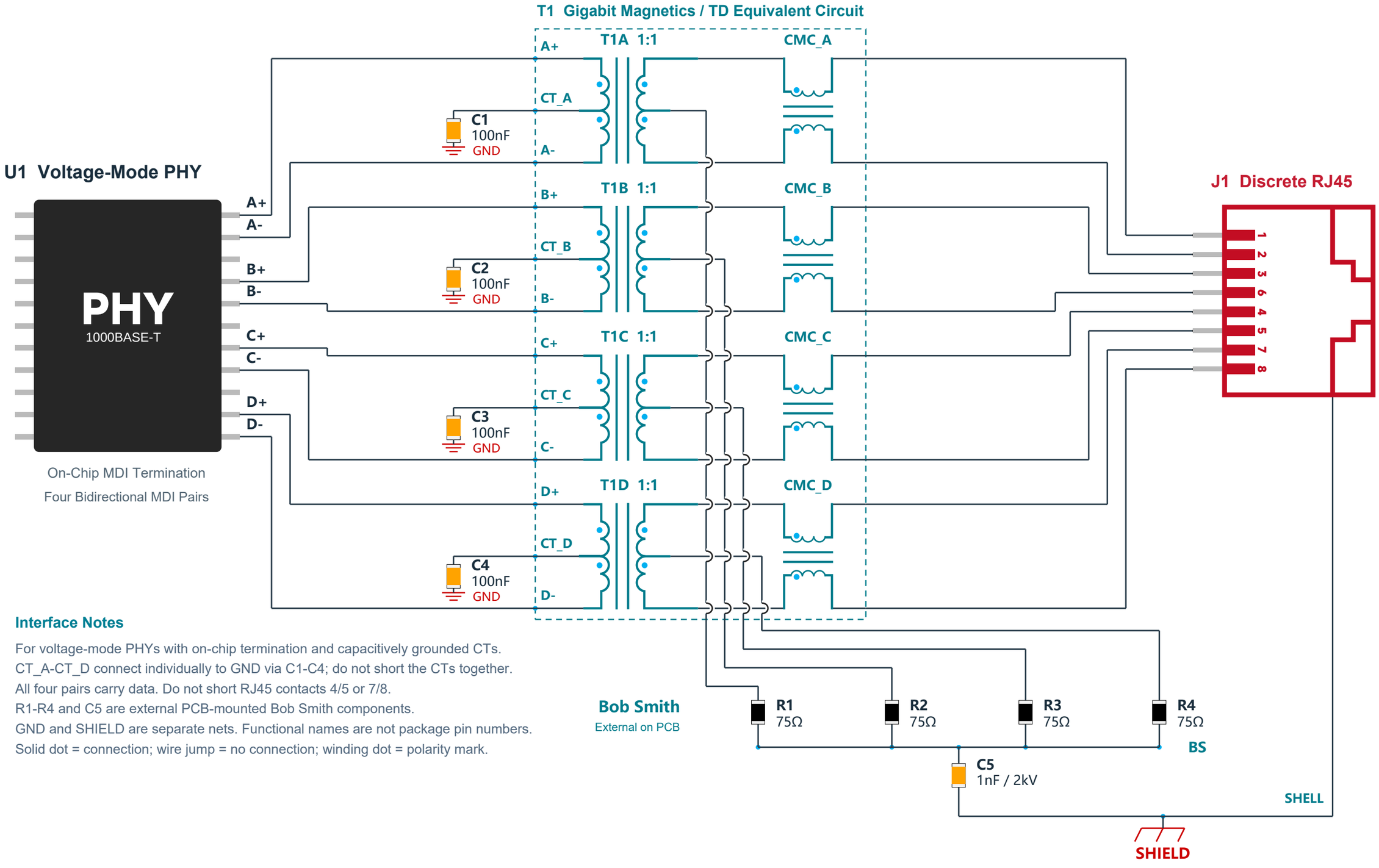


Interface Notes

For voltage-mode PHYs with on-chip termination and capacitively grounded CTs.
CT_A-CT_D connect individually to GND via C1-C4; do not short the CTs together.
All four pairs carry data. Do not short RJ45 contacts 4/5 or 7/8.
R1-R4 and C5 are external PCB-mounted Bob Smith components.
GND and SHIELD are separate nets. Functional names are not package pin numbers.
Solid dot = connection; wire jump = no connection; winding dot = polarity mark.

1000BASE-T Network Interface & Gigabit Magnetics & Voltage-Mode PHY

Non-PoE | Four bidirectional MDI pairs | Discrete RJ45 + external TD magnetics



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MDI reference circuit: map functional terminal names to the actual package pins of the selected PHY, magnetics and RJ45.

Component Parameters, Connections and Design Basis

Independently designed circuit, supported by Gigabit PHY and magnetics interface documentation. Generic component names are used; example ICs identify the technical sources only.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / Voltage-Mode PHY	1 device	Limited to Gigabit PHYs with on-chip MDI termination and capacitively grounded PHY-side CTs. No duplicate 49.9Ω termination or external CT supply is added. This connection is not universally applicable to all voltage-mode PHYs.	E1 pp.114-115; E2 pp.3-4; E4 p.3
C1-C4 / 100nF	4, outside T1	Connect CT_A/CT_B/CT_C/CT_D individually to GND, providing an AC common-mode return while blocking DC in each branch. Keep the four CTs independent. Place each capacitor close to its pin; do not combine them into one capacitor.	E1 p.115, Fig.9-2; E2 p.4, §4.2
T1A-T1D / 1:1	4 channels, inside T1	Four isolation transformers carry differential signals A/B/C/D. Each PHY-side CT connects to GND only through its own capacitor; each cable-side CT connects to its own 75Ω resistor. Verify inductance, insertion loss, return loss, crosstalk and insulation against the selected PHY.	E1 pp.115-116; E3 p.5, Fig.3
CMC_A-CMC_D	4 channels, inside T1	Each two-winding CMC is in series with both cable-side data lines to suppress common-mode interference. The CMC and isolation transformer form a TD channel without an autotransformer winding. Bob Smith termination is taken from the transformer cable-side CT.	E3 pp.4-5, Fig.3
R1-R4 / 75Ω	4, outside T1	Each cable-side CT connects to the common BS node through its own 75Ω resistor, forming common-mode termination. Do not short the four CTs together before the resistors. These 75Ω resistors are not in series with the main differential signal path.	E1 p.115, Fig.9-2; E2 p.4, §4.2
C5 / 1nF, 2kV	1, outside T1	C5 AC-couples BS to SHIELD and blocks DC. Values follow the manufacturer examples. Specify the actual component voltage rating behind the 2kV label and verify system insulation tests; the label does not directly mean 2kVac or a surge immunity level.	E1 p.115, Fig.9-2; E2 p.4, §4.2
J1 / Discrete RJ45	1, no magnetics	Map A to 1/2, B to 3/6, C to 4/5 and D to 7/8, preserving polarity within each pair. All four pairs carry 1000BASE-T data; do not short contacts 4/5 or 7/8. Connect the metal shield directly to SHIELD.	E1 p.115, Fig.9-2; E2 p.4, Fig.4-1
GND / SHIELD	Two separate nets	C1-C4 return to the PHY circuit ground, GND. The other side of C5 and the RJ45 shell connect to SHIELD. Any coupling components and connections to chassis or protective earth (PE) depend on the enclosure, EMC and insulation requirements.	E1 p.115, Note D; E2 p.4, §8.2

Technical Sources and Scope of Use

E1 · Texas Instruments DP83867IR/CR, SNLS484J, revised June 2026, pp.114-116, Fig.9-2: on-chip termination, four independent 0.1µF capacitors, pair mapping and 75Ω + 1nF/2kV termination.

E2 · Microchip KSZ9131MNX Hardware Design Checklist, DS00003371A, 2020, pp.3-4, §§4.1/4.2, Fig.4-1: no external termination or bias, independent CT capacitors and a shared Bob Smith capacitor.

E3 · Microchip / Microsemi ENT-AN0098 / VPPD-01740, Rev.2.2, June 2018, printed pp.4-5, Fig.3 (PDF pp.6-7): isolation transformer with a cable-side two-winding CMC, and cable-side CT termination location.

E4 · Motorcomm YT8511 Application Notes, V1.2, p.3, "MDI Interface." Public reproduction of manufacturer-attributed material, used to cross-check voltage-mode output, on-chip termination and 100nF to GND. Confirm the current version with the manufacturer when selecting parts.

PCB Implementation

Route all four MDI pairs for 100Ω differential impedance; control within-pair skew and stub length. Place CT capacitors close to their pins with local GND returns. Preserve the magnetic isolation region and follow the PHY and magnetics manufacturers' power/ground copper layout rules. Bob Smith termination is for common-mode termination, not ESD or surge clamping.

Scope: a non-PoE MDI interface reference. After selecting the PHY, magnetics and port protection, recheck values, package pin mapping and system grounding, and perform link, MDI, EMC and insulation tests. Schematic and document review does not replace hardware validation.