# Circuit Design

## Fast Ethernet Capacitive ChipLAN & Voltage-Mode PHY

**100 m Target / Validation Edition**

### Design Overview

**1. Design Target and Conditions**

A non-PoE external Ethernet port with a target cable length of up to 100 m. Use a voltage-mode PHY supporting capacitive coupling and on-chip termination. This is a validation circuit; 100 m interoperability and full standards compliance remain unconfirmed.

**2. Signal Coupling and Protection**

Each TD±/RD± line has a series capacitor, C1-C4 (33nF reference value), for DC-blocking coupling. D1-D4 are low-capacitance TVS devices matched to the PHY, connected from each line to GND on the PHY side of the capacitors. These are signal-coupling capacitors, not power decoupling capacitors.

**3. Common-Mode Filtering and Port Connections**

L1/L2 are inserted in the two differential pairs. In normal MDI mode, TX± connects to RJ45 contacts 1/2 and RX± to 3/6. Contacts 4, 5, 7 and 8 are individually NC. No CT supply, external 49.9Ω pull-up termination or Bob Smith network is shown.

**4. Grounding and Isolation**

Connect the metal shell to SHIELD and keep circuit GND separate. Select C1-C4 and cross-barrier clearances against the port isolation test; capacitor nameplate voltage alone is insufficient. Autotransformer windings do not provide isolation and are omitted.

**5. PCB Implementation**

Route MDI for 100Ω differential impedance with symmetric pair layout and short TVS ground returns. Complete PHY power, clock, reset, MAC and LED circuits separately. Original product images are retained; confirm compatibility when selecting parts.

### Product Illustrations



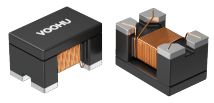
- SYT561188-AB1A3DY1027



- SYT60S1188-AB1A6DY1008

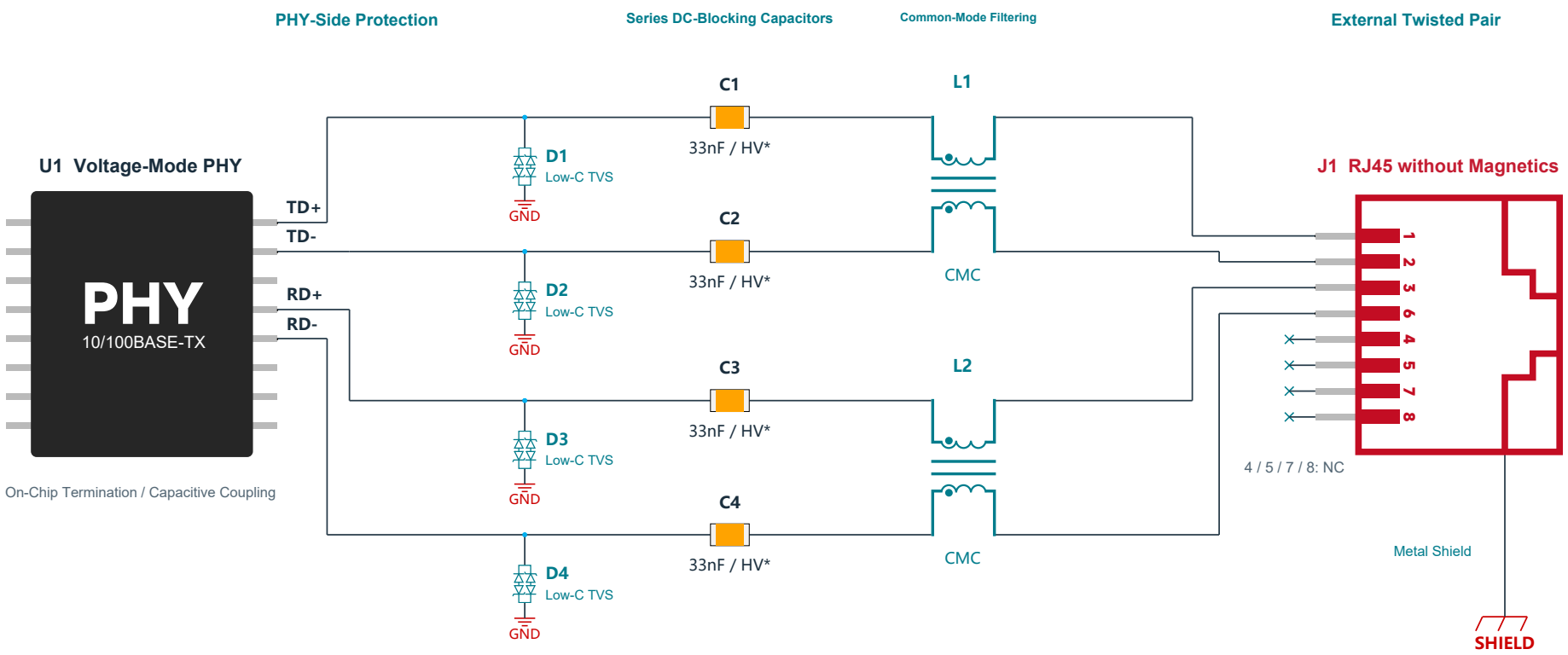


- WHLC-3216A Series



- WHLC-2012A Series

### Reference Schematic




C1-C4 are series signal DC-blocking capacitors. D1-D4 are on the PHY side, each returning to circuit GND.

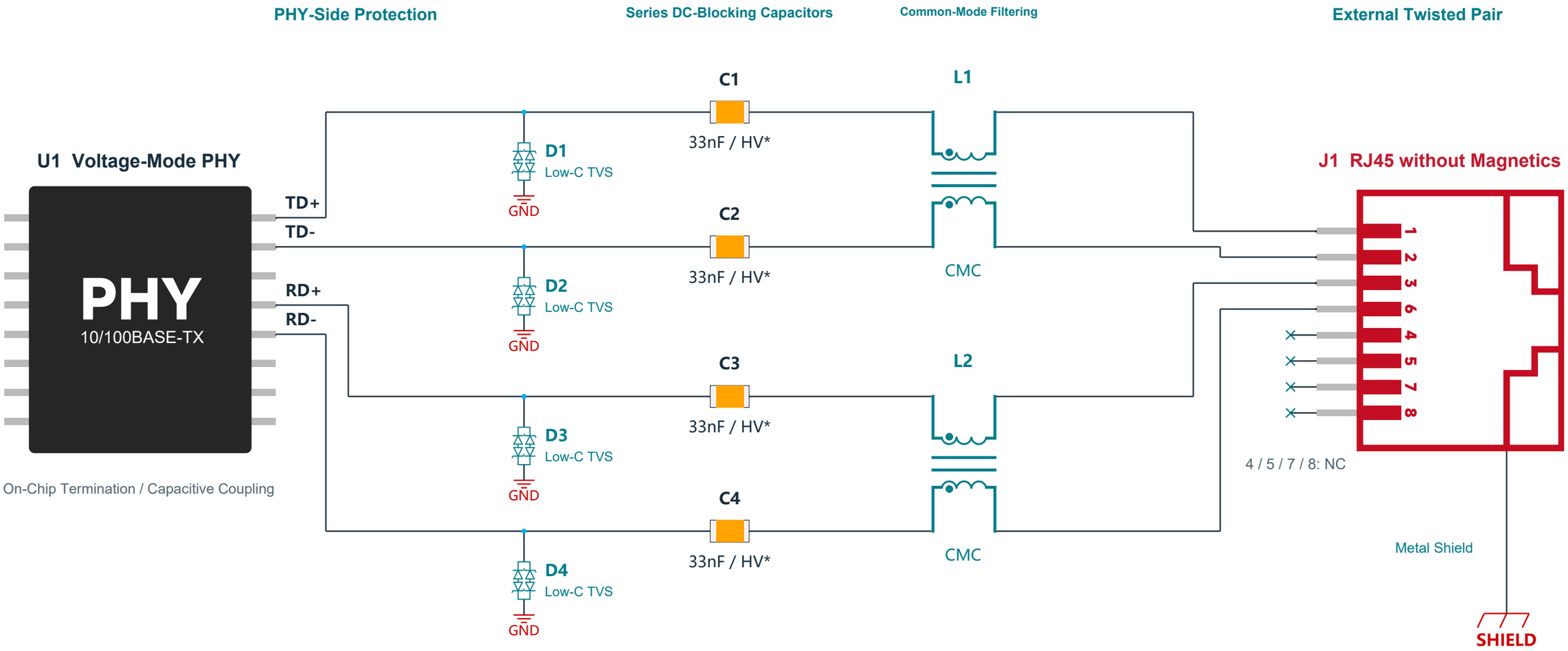
HV*: verify isolation rating, test conditions and package spacing for the system. Keep SHIELD and GND separate.

**100 m is a validation target. Target-length interoperability, isolation and EMC have not been verified.**

For component selection and prototype validation. 100 m interoperability, port isolation and EMC remain unverified; this is not a production release.

# Fast Ethernet Capacitive ChipLAN & Voltage-Mode PHY

Non-PoE | External cable | Voltage-mode PHY with on-chip termination and capacitive coupling | 100 m target not yet validated




C1-C4 are series signal DC-blocking capacitors. D1-D4 are on the PHY side, each returning to circuit GND.

HV*: verify isolation rating, test conditions and package spacing for the system. Keep SHIELD and GND separate.

**100 m is a validation target. Target-length interoperability, isolation and EMC have not been verified.**

Functional names are not package pins; RJ45 numbers are cable contacts. Dot = connection; wire jump = no connection. Keep all NC contacts separate.

# Capacitive Coupling Basis and the 100 m Validation Limit

A prototype candidate based on manufacturer capacitive-coupling architectures. The 100 m target is user-defined; part selection, link partners and system test conditions remain unresolved. This design cannot be marked as meeting ordinary 100 m Ethernet-port requirements.

| Component / Value | Qty / Location | Design Rationale and Constraints | Source |
|---|---|---|---|
| U1 / Voltage-Mode PHY | 1 device; functional MDI pins | Select an implementation supporting capacitive coupling and on-chip termination. No CT supply or external pull-up termination is shown. Generic functional pins cannot replace the selected part's package mapping and register configuration. | [1][2]; conditional architecture |
| C1-C4 / 33nF, HV* | 4; one in series with each line | Use the manufacturer DC-blocking value as a validation starting point. Capacitors must be nonpolar and pair-matched. Verify tolerance, dielectric, isolation rating, test duration, leakage current and spacing. A DC voltage rating is not AC isolation capability; ordinary low-voltage MLCCs are not substitutes. | [1] Fig.9-3; [2] Fig.39; [3] capacitor selection |
| D1-D4 / Low-C Bidirectional TVS | 4 channels; PHY side to GND | Each MDI line connects through a TVS to circuit GND before its series capacitor. Working voltage must cover signal and common-mode ranges. Coordinate clamping, dynamic resistance, junction capacitance and residual voltage with the PHY. Functional equivalents are shown; parts and protection levels remain undefined. | [2] Fig.39; [3] Protection |
| L1 / L2 / Two-Line CMC | 2 groups; between capacitors and RJ45 | Provide common-mode filtering for the two pairs. Select impedance curves, insertion loss, return loss and balance suitable for 10/100M. These are not series differential-mode inductors, and a 2012 package designation alone is insufficient for selection. | [2][3]; placement is an engineering implementation |
| J1 / SHIELD / RJ45 without Magnetics | 1; cable side | Data pairs use 1/2 and 3/6; all other contacts are individually open. Connect the shell to SHIELD and keep GND separate. No unverified unused-pair termination or GND-SHIELD coupling network is added. | [2] Fig.39; functional pin mapping |
| Autotransformer / Not Fitted | 0 devices | No manufacturer connection matching the selected capacitive-coupling architecture has been established for this design. An autotransformer does not provide primary-to-secondary isolation. Grounding its tap directly would establish a DC path from the cable to circuit GND. | [1][2] schematics; deduction from DC connectivity |
| 100 m Target / Validation Pending | Complete link; not a component rating | Manufacturer long-cable experiments cannot be generalized across PHYs, link partners and environments. Validate 10M/100M, auto-negotiation and MDI-X, short/long cables, link drops/errors, transmit waveforms and return loss. Perform isolation and EMC tests separately. | [2][3][4]; not hardware-tested |

## Manufacturer Sources and Scope of Use (click to open)

**[1] · TI** DP83826 Datasheet, SNLS647I, August 2025, p.1 and pp.95-97, Fig.9-3. Basis for voltage-mode MDI and four 33nF series DC-blocking capacitors. This does not establish 100 m or EMC compliance for this schematic.

**[2] · ADI** ADIN1200 Rev.B, pp.42-43, Fig.39; pp.75-76, Table 98. Basis for on-chip termination, PHY-side TVS, CMC recommendations and short-cable scope. Capacitive coupling with this device requires disabling receive zero-power termination.

**[3] · ADI** ADIN1300 and ADIN1200 with Capacitive Coupling, February 11, 2021, Protection / Configurations / Evaluation. Long-cable results are for ADIN1300 with capacitive coupling at both ends under nominal conditions; they do not replace validation of a generic Fast Ethernet port with ordinary link partners.

**[4] · TI** TLK110 Ethernet PHY Transformerless Operation, SLLA327, September 2012, pp.3, 6-8. The 120 m result belongs only to its specified TLK110 circuit, and the document states that it is not fully IEEE-compliant. Its pull-up termination is not adopted here.

## Conditions to Resolve Before Production

Select the actual PHY, CMCs, TVS devices, DC-blocking capacitors and RJ45. Validate 0.5/1/10/50/100 m links and common transformer-coupled partners at temperature and supply corners. Define isolation test nodes, AC/DC method, amplitude and duration; define EMC levels, coupling and acceptance criteria. If ordinary 100 m Ethernet-port requirements must be met directly, prefer a magnetic-isolation architecture supported by corresponding validation evidence.

Schematic text and connection data have been checked. No native EDA ERC, 100 m prototype testing, isolation testing or EMC certification has been performed.