Circuit Design

10/100BASE-T Integrated Network Interface & Current-Mode PHY

Design Overview

1. Scope

For non-PoE 10BASE-T/100BASE-TX interfaces using external PHY termination, where both PHY-side center taps permit a bias supply. VBIAS is typically 3.3V; confirm its actual value from the PHY specification.

2. PHY-Side Termination and Bypass

Connect TD±/RD± to J1 TX±/RX±, respectively. R1-R4 (49.9Ω ±1% each) pull each signal line to VBIAS for termination and bias. C1/C2 (100nF each) bypass locally to GND. CT_TX/CT_RX connect to VBIAS; C3/C4 (100nF each) bypass to GND close to the respective CTs.

3. Isolation and Cable-Side Connections

J1 contains two 1:1 isolation transformers and CMCs. In normal MDI mode, TX± connects to RJ45 cable contacts 1/2 and RX± to 3/6. Automatic pair exchange requires PHY Auto-MDIX support. Preserve polarity within each pair.

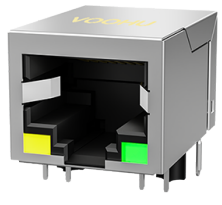
4. Bob Smith Termination and Shield

TX/RX cable-side CTs and unused pairs 4/5 and 7/8 connect through Ra/Rb/Rc/Rd (75Ω each) to BS. BS connects via internal Cb (1nF) and BS_RET to SHIELD; do not duplicate the network externally. SHELL shares SHIELD. Define GND, SHIELD and protective earth (PE) connections at system level.

5. Insulation and Implementation

HV*: TI recommends at least 2kV for Cb; verify voltage-rating type and test conditions against the part specification. Bob Smith termination does not replace surge protection. Place R1-R4 and C1/C2 near the PHY; route MDI for 100Ω differential impedance. Design PHY power, clock, reset and configuration separately. Product images show appearance only; verify internal circuits and actual PCB pins.

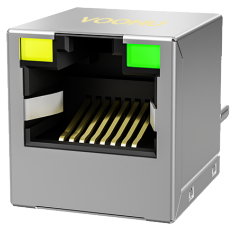
Product Illustrations



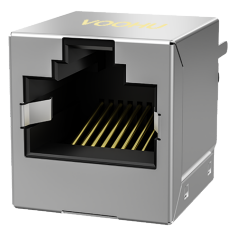
- SYT111B002-BA2A1D



- SYT111B002-GWA1D

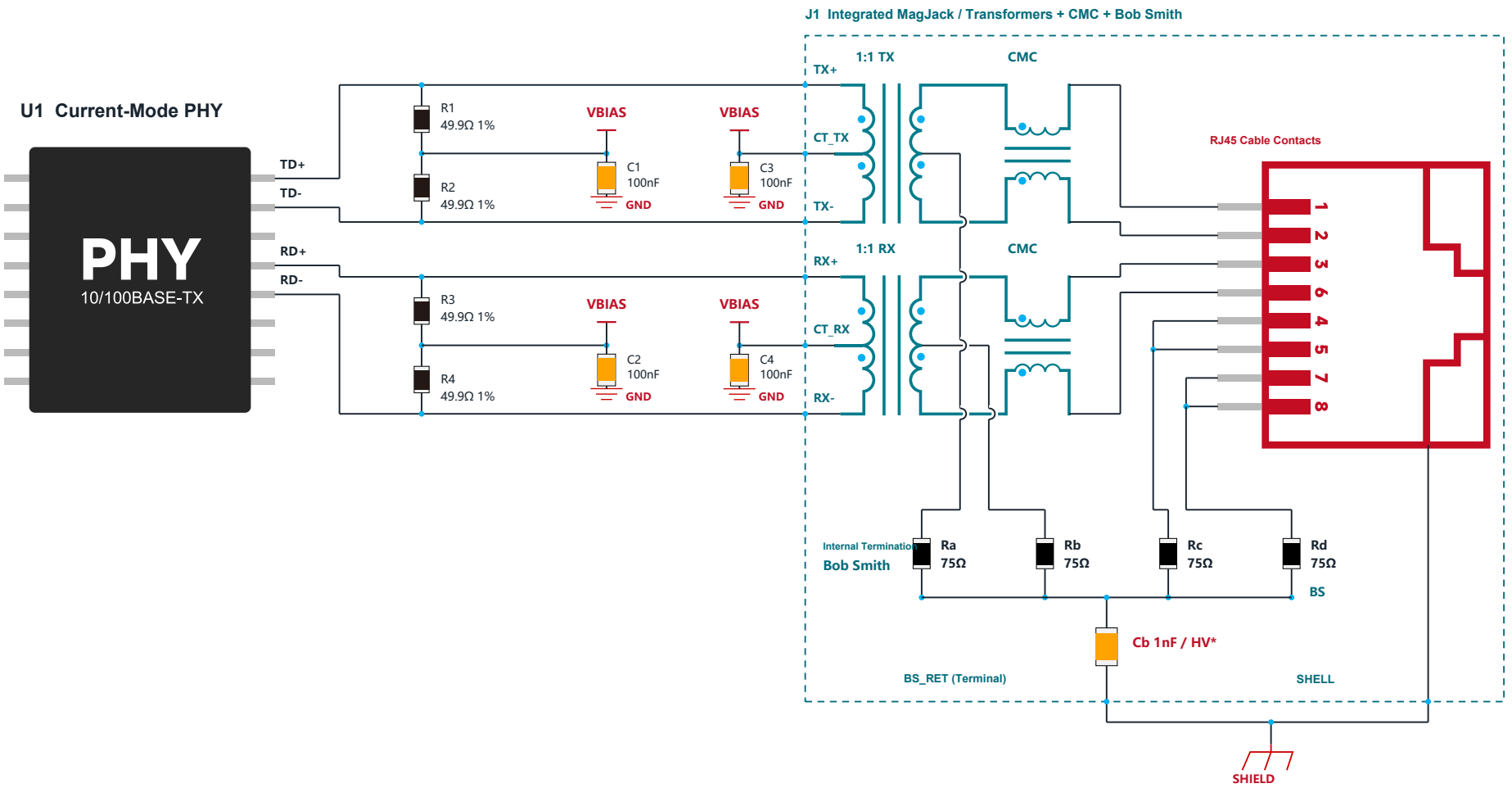


- SYT511B048-AA1A8D



- SYT511B048-GWA8D

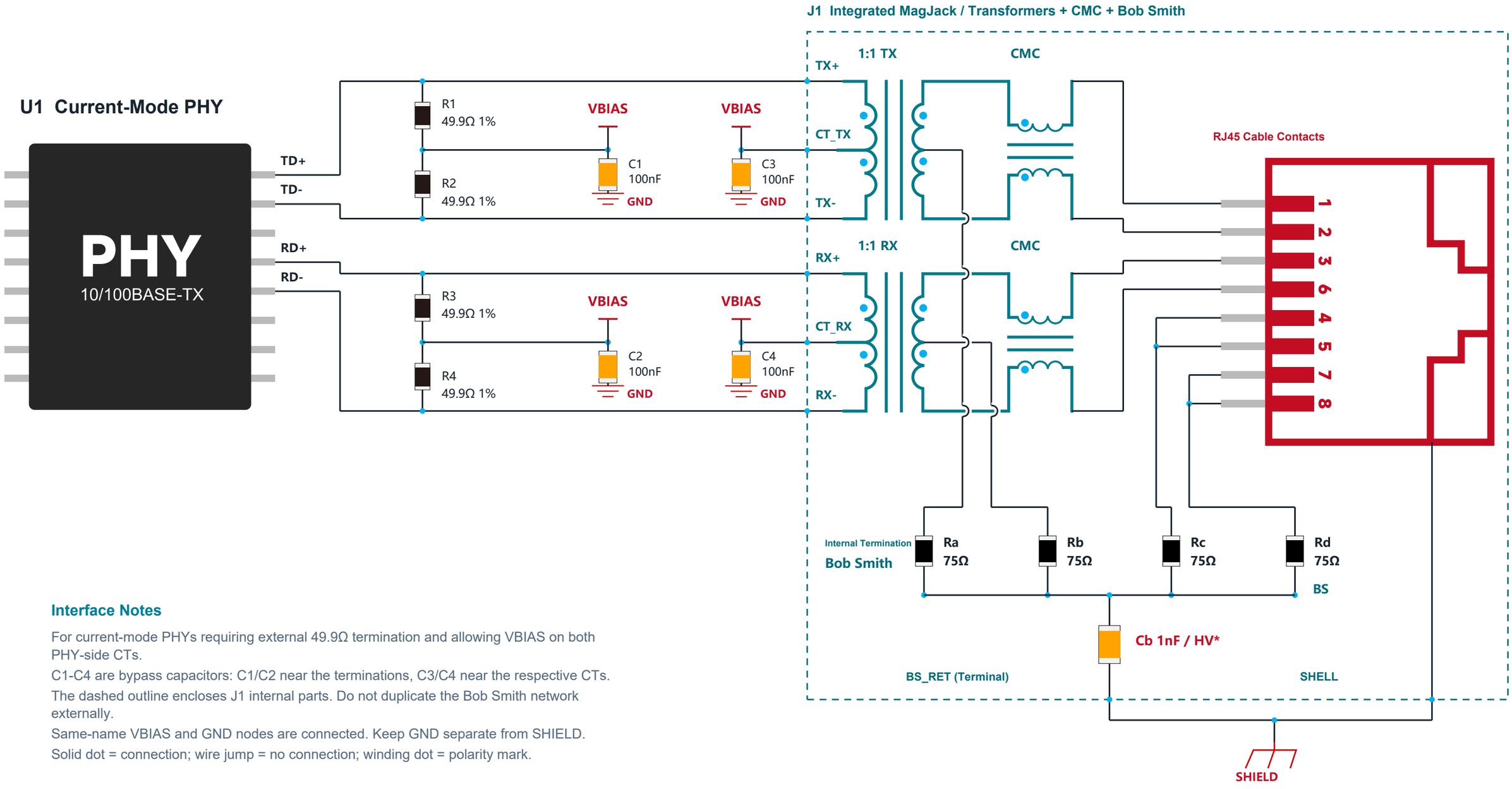
Reference Schematic



Note: Reference design only. Adapt the final circuit to the actual application. Contact us for further technical support.

10/100BASE-T Integrated Network Interface & Current-Mode PHY

Non-PoE | External termination; both PHY-side CTs connect to bias | Integrated MagJack



Interface Notes

For current-mode PHYs requiring external 49.9Ω termination and allowing VBIAS on both PHY-side CTs.

C1-C4 are bypass capacitors: C1/C2 near the terminations, C3/C4 near the respective CTs.

The dashed outline encloses J1 internal parts. Do not duplicate the Bob Smith network externally.

Same-name VBIAS and GND nodes are connected. Keep GND separate from SHIELD.

Solid dot = connection; wire jump = no connection; winding dot = polarity mark.

HV*: TI recommends a Cb rating of at least 2kV. Verify voltage type, test conditions and module insulation. Map functional names to the selected parts' actual PCB pins.

Component Parameters, Connections and Design Basis

Based on original 10/100 Mb/s PHY and magnetics interface documentation. Component names remain generic; example ICs identify technical sources only.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / Current-Mode PHY	1, outside J1	Limited to a 10/100 Mb/s architecture with external termination and both PHY-side CTs connected to bias. Confirm VBIAS and the complete power, clock, reset and configuration requirements for the selected PHY.	E3 pp.68-69; E2 p.4
R1-R4 / 49.9Ω ±1%	4, outside J1	Each TD± and RD± line connects to VBIAS through its own resistor for termination and bias. Do not connect the common termination node directly to GND. Place R1-R4 close to the PHY.	E3 p.69, Fig.7-2; E2 p.4, Fig.3-4
C1, C2 / 100nF	2, outside J1	Connect the VBIAS nodes of the two termination networks to GND, respectively, providing local bypass paths for high-frequency current. Place each capacitor close to its associated termination resistors.	E3 p.69, Fig.7-2; E2 p.4, §3.2
C3, C4 / 100nF	2, outside J1	CT_TX and CT_RX connect directly to VBIAS, each with a local 100nF bypass to GND. Retain the manufacturer's per-channel arrangement; sharing a net does not justify omitting local bypass capacitors.	E3 p.69, Fig.7-2; E2 p.4, §3.2
TX/RX Transformers / 1:1	2, inside J1	Transfer differential signals and isolate the PHY from the cable. PHY-side CTs connect to VBIAS; each cable-side CT connects through 75Ω to BS. Match turns ratio, winding polarity and magnetic characteristics to the selected PHY and module.	E3 p.69, Fig.7-2; E4 p.5
CMC / Common-Mode Chokes	2, inside J1	Located on the transformer cable side, with windings in series with both data lines. Common-mode impedance suppresses common-mode interference. Module insertion loss, return loss, balance and common-mode response must still meet interface requirements.	E1 p.7, §2.4; E4 p.5
Ra-Rd / 75Ω	4, inside J1	Ra/Rb connect the TX/RX cable-side CTs to BS. Contacts 4/5 are shorted before Rc, and 7/8 before Rd. All four branches reach BS through their own 75Ω resistors. This arrangement is limited to the non-PoE 10/100 Mb/s scope shown.	E1 p.6, §2.3; E4 p.5
Cb / 1nF, HV*	1, inside J1	BS connects through Cb and BS_RET to SHIELD, providing a high-frequency common-mode return while blocking DC. TI recommends at least 2kV. Verify voltage type, test conditions and the internal capacitor specification separately; this is not a surge immunity rating.	Value/internal: E4 p.5; voltage guidance: E1 p.6
J1 / RJ45 and Shield	1 integrated module	Normal MDI: TX+/- maps to contacts 1/2 and RX+/- to 3/6. Auto-MDIX requires PHY support. SHELL and BS_RET connect to the same SHIELD outside the module. Cable contact numbers are not PCB pin numbers.	E3 p.69, Fig.7-2; E4 p.5; E1 p.7
GND / SHIELD	Two reference nets	C1-C4 connect to circuit GND. The shield side of Cb and the metal shell connect to SHIELD. No GND-SHIELD coupling network is shown. Chassis and PE connections are determined by the system design.	E1 pp.6-7; E4 p.5 (structure)

Technical Sources and Scope of Use

E1 · Texas Instruments AN-1469 / SNLA079D, Rev.D, April 2013, pp.4-7 and p.13: termination layout, 100Ω differential routing, 75Ω + 1000pF common-mode termination and a capacitor rating recommendation of at least 2kV.

E2 · Texas Instruments DP83848 to DP83826A Hardware Rollover Document, SDAA089, September 2025, p.4, §3.2 / Fig.3-4: current-mode external termination, CT bias connection and 100nF per channel.

E3 · Texas Instruments DP83848C/I/VYB/YB, SNLS266E, March 2015, pp.68-69, Fig.7-2: 49.9Ω termination, four 0.1µF capacitors and 1:1 magnetics for a 10/100 Mb/s interface. Applicability must match the selected PHY.

E4 · Pulse Electronics J403.K, August 2012, p.5, internal diagrams for J0011 and related families: cable-side CMCs, 4 × 75Ω and an internal 0.001µF capacitor. The public copy of the manufacturer document supports this structure. That page does not specify Cb voltage rating or establish compatibility of the displayed product models.

Implementation Requirements

Route MDI for 100Ω differential impedance; place termination and CT capacitors locally and preserve the module isolation boundary. After component selection, verify internal circuitry, PCB pins and supply conditions. Bob Smith termination provides common-mode termination and does not replace ESD or surge protection.

Scope: a non-PoE reference design for a specific current-mode MDI architecture. After selecting the PHY and MagJack, verify ratings, PCB pins and system grounding, then validate link operation, EMC and insulation. Schematic and text review cannot replace prototype tests.