Circuit Design

10/100BASE-T Surge and ESD Protection & Current-Mode PHY

Design Overview

1. Scope

Non-PoE 10BASE-T/100BASE-TX; discrete RJ45 with external TD magnetics and reliable chassis/PE. For current-mode architectures with external 49.9Ω termination on each line and both PHY-side CTs connected to a bias supply.

2. Termination, Bias and Bypass

R1-R4 are 49.9Ω ±1%; each MDI line connects through its resistor to VBIAS. C1/C2 are 100nF each, close to the termination. CT_TX and CT_RX share VBIAS; C3/C4 (100nF each) bypass locally to GND. Set VBIAS per the selected PHY.

3. Magnetics and Cable Connections

T1 has two 1:1 isolation transformers and cable-side CMCs. In normal MDI mode, TX± connects to RJ45 contacts 1/2 and RX± to 3/6. Join unused contacts 4/5 together and 7/8 together. Pair swapping requires PHY support.

4. Staged Protection

D1/D2 are PHY-side low-capacitance bidirectional differential TVS devices. G1/G2 connect cable-side CTs to SHIELD; G3/G4 connect the two unused-pair groups to SHIELD. All take-off points precede the 75Ω resistors. Connect SHIELD to reliable chassis/PE.

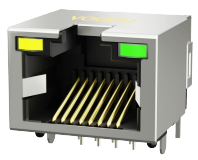
5. Common-Mode Termination and Grounding

Each of four branches passes through 75Ω to BS, then through C5 (1nF high-voltage capacitor) to SHIELD. The metal shell shares SHIELD; GND remains separate. Coordinate TVS, GDT, magnetics and C5 selection with protection and insulation targets. See page 3 for the technical basis.

Product Illustrations



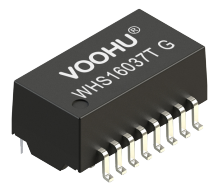
- SYT561188-AB1A3DY1027



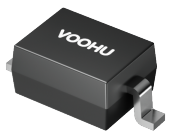
- SYT60S1188-AB1A6DY1008



- WHS16013LF



- WHS16037TG (Industrial Grade)

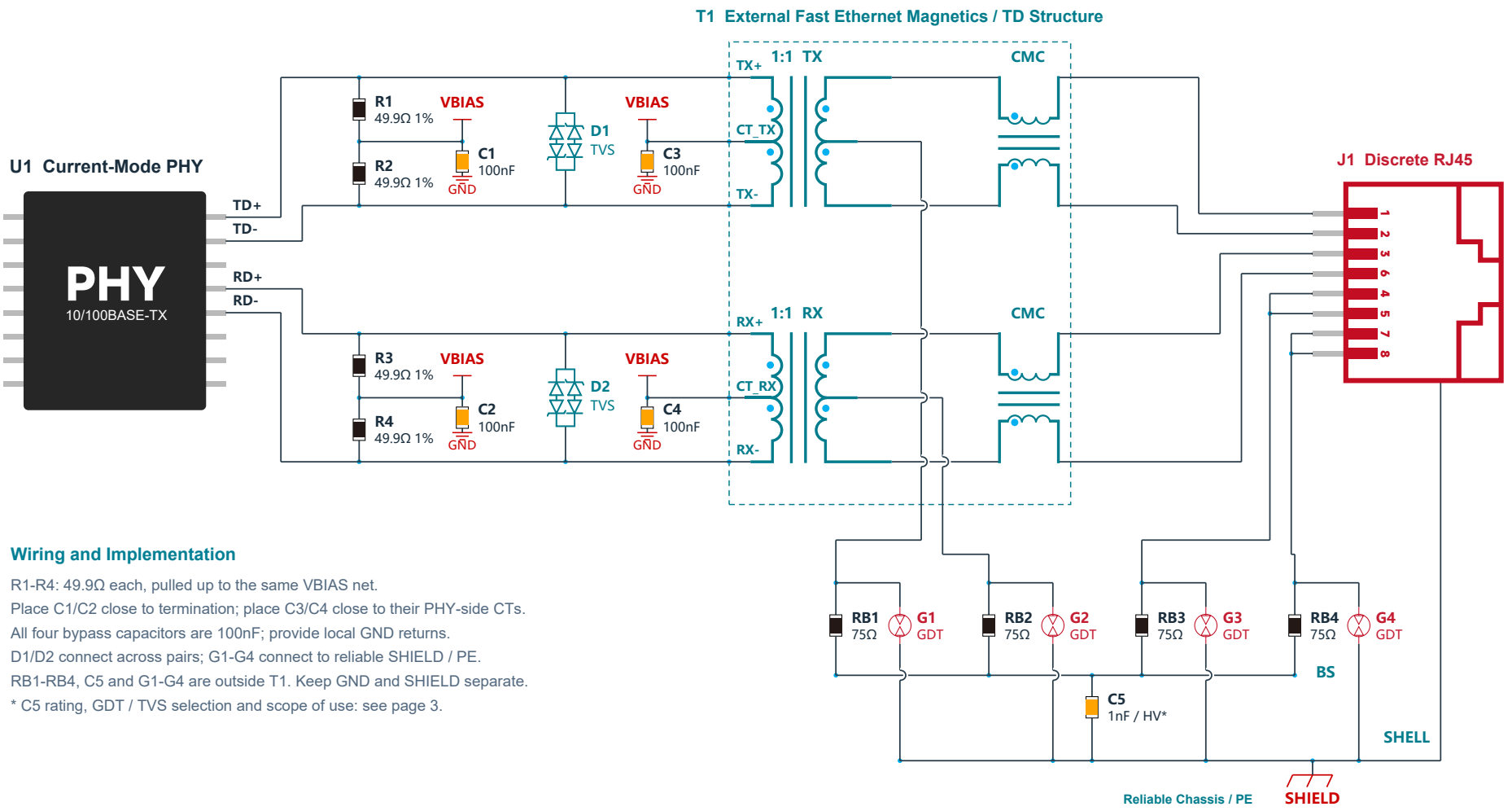


- WHTA3V30P8B



- WHGD090V1P0B

Reference Schematic



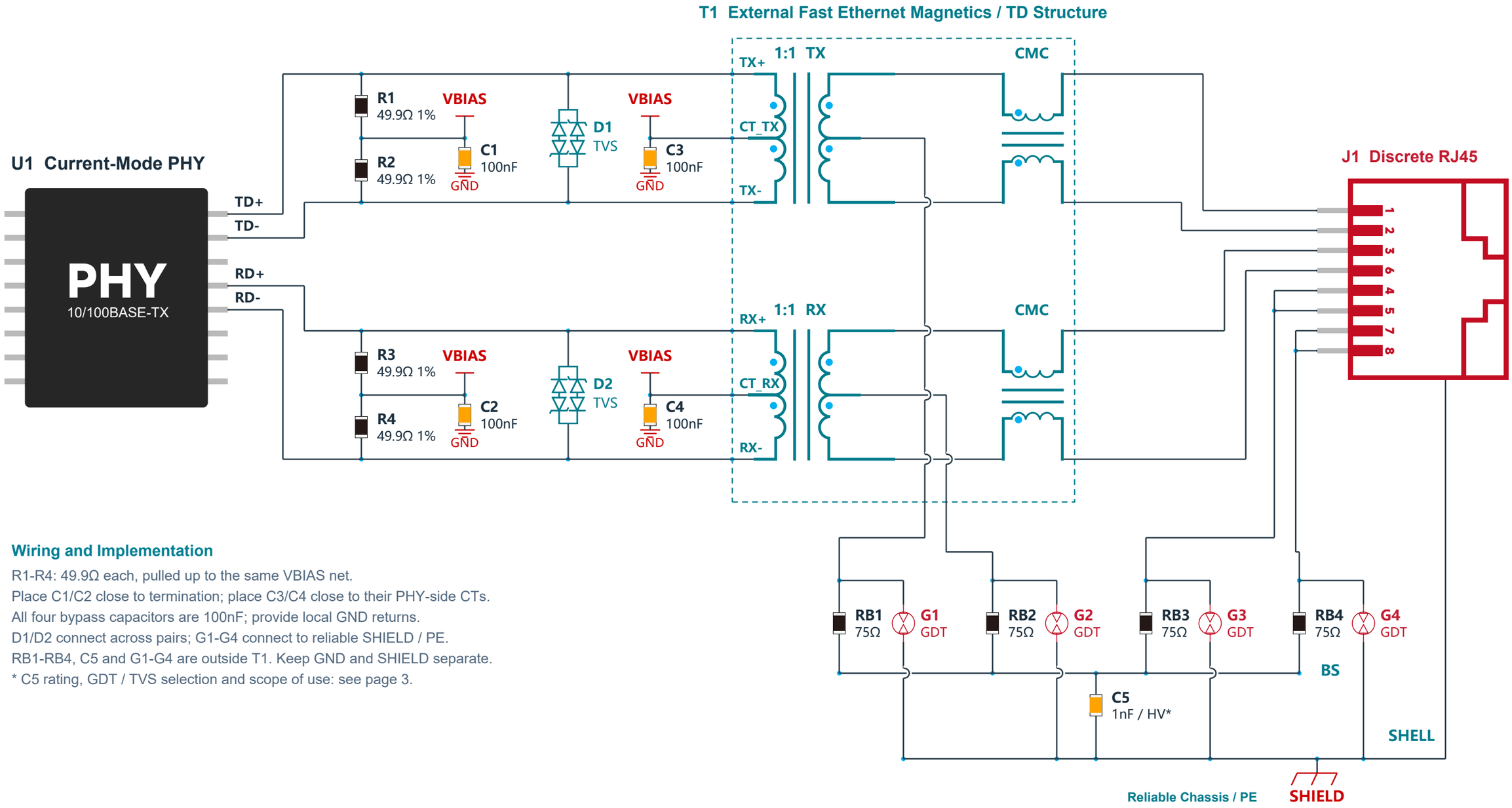
Wiring and Implementation

R1-R4: 49.9Ω each, pulled up to the same VBIAS net.
Place C1/C2 close to termination; place C3/C4 close to their PHY-side CTs.
All four bypass capacitors are 100nF; provide local GND returns.
D1/D2 connect across pairs; G1-G4 connect to reliable SHIELD / PE.
RB1-RB4, C5 and G1-G4 are outside T1. Keep GND and SHIELD separate.
* C5 rating, GDT / TVS selection and scope of use: see page 3.

Reference circuit for design and component selection. Final connections, component parameters and protection performance depend on actual selection and system validation.

10/100BASE-T Surge and ESD Protection & Current-Mode PHY

10BASE-T / 100BASE-TX | Non-PoE | External pull-up termination / CT bias | Reliable chassis / PE



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Functional names are not package pins; RJ45 numbers are cable contacts. Solid dot = connection; winding dot = polarity mark; wire jump = no connection. Protection selection: page 3.

Component Functions, Sources and Validation Conditions

A TI Fast Ethernet current-mode interface example is combined with TVS and GDT protection. The table distinguishes manufacturer evidence from engineering design. Protection parts and test conditions remain undefined; the combined circuit has no established system protection level.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / R1-R4	1 PHY; 4 resistors	Each TD±/RD± line connects through 49.9Ω ±1% to VBIAS, giving approximately 100Ω differential termination. Limited to this external-termination architecture. If the PHY has on-chip termination or different CT rules, redesign to its manufacturer guidance; the label "current-mode" is insufficient.	E1 Figs.3-4; E2 §2.1
C1-C4 / VBIAS	4 × 100nF	C1/C2 are close to the two termination networks; C3/C4 are close to the two PHY-side CTs. All bypass VBIAS to GND. Local placement is still required on a shared VBIAS net. The DP83848 example uses 3.3V; the generic schematic does not fix the voltage.	E1 p.4; E2 Fig.2
T1 / CMC	2 channels; TD structure	1:1 isolation transformers with cable-side common-mode chokes; preserve polarity. Verify inductance, insertion loss, return loss, balance and insulation for the selected PHY. The GDT current path includes windings/CMCs, whose pulse withstand capability must be checked.	Basic interface: E2; pulse coordination: E5
D1 / D2	2 differential protection channels	Low-capacitance bidirectional TVS devices connect across PHY-side P/N, close to the magnetics with short branches. VRWM must cover the normal differential swing. Clamping, response and energy at the actual surge current must satisfy the PHY transient limits. This branch does not directly clamp pair common-mode voltage.	E3 Fig.4; E5 pp.6-9
G1-G4 / GDT	4 branches, outside T1	G1/G2: cable-side CT → SHIELD. G3/G4: unused-pair group → SHIELD. All connect before 75Ω. Verify impulse sparkover, current capacity, residual voltage and port-to-chassis insulation tests. This topology does not guarantee protection of magnetics against differential surge.	CT concept: E4 p.8; unused-pair extension: engineering design
RB1-RB4 / C5	4 × 75Ω + 1nF	Two CTs and two unused-pair groups each pass through 75Ω to BS, then through C5 to SHIELD. This is common-mode termination, not a replacement for TVS/GDT protection. HV* uses ≥2kV as a reference; verify AC/DC rating and pulse capability against actual insulation needs, and check 75Ω pulse stress.	E2 pp.4, 6; component stress: E5
J1 / Shield / Ground	1 discrete RJ45	TX → 1/2; RX → 3/6. In this non-PoE design, 4/5 and 7/8 each form a group. SHELL, GDTs and C5 return to reliable chassis/PE; GND stays independent. Complete connector pin mapping, LEDs and PHY power, clock and reset for the selected parts.	E2 §§2.3-2.4; grounding condition confirmed by user

Manufacturer Sources and Scope of Use (click to open)

E1 · Texas Instruments — SDAA089, September 2025, p.4, §3.2 / Figs.3-4. DP83848 Fast Ethernet current-mode example: 49.9Ω per line to AVDD33 and local 100nF at termination and each CT. Used only for the restricted architecture shown; the example bias is 3.3V.

E2 · Texas Instruments — AN-1469 / SNLA079D, April 2013, pp.4-7, Fig.2 and §§2.1-2.4: magnetics, routing, common-mode termination and shielding. C5 follows the p.6 text recommendation of 1000pF and ≥2kV. Fig.2 shows 1500pF; it is not treated as the sole mandatory value.

E3 · Semtech — Ethernet Protection Methodology, February 19, 2020, Fig.4. Adopts the PHY-side across-pair TVS method. Select clamping and energy capability for the signal, PHY limits and actual pulse. The example test results do not establish this design's protection level.

E4 · Littelfuse — General Port Protection, 2024, pp.8, 10. p.8 is a PoE++ CT-to-ground protection example; only the local GDT discharge concept is used. p.10 illustrates staged Ethernet protection. Adapting it to non-PoE and extending it to unused pairs is an engineering combination.

E5 · Bourns — Ethernet and PoE Protection Technical Article, December 2006, pp.6-9. GDT triggering can increase PHY-side pulse stress, requiring coordinated TVS and magnetics selection. Only this coordination principle is adopted, not its historical test standards or levels.

PCB Implementation and Protection Validation

Use 100Ω differential MDI routing. Place R1-R4 and C1/C2 close to the PHY, C3/C4 close to their CTs, and D1/D2 close to the magnetics. Keep GDT-to-PE paths short and wide, separated from the PHY area. Define IEC 61000-4-2/-4-5 levels, waveforms, coupling network, source impedance and acceptance criteria, then validate the link, residual voltage, pulse stress and insulation. No fixed kV performance is promised. PoE, direct lightning strikes and sustained power-frequency faults are outside scope; displayed products are not confirmed matches.

Schematic text and connection data have been checked. No native EDA ERC, prototype protection testing or system certification has been performed.