Circuit Design

10/100BASE-T Network Interface & Fast Ethernet Magnetics & Voltage-Mode PHY

Design Overview

1. Scope

Non-PoE; discrete RJ45 with external Fast Ethernet magnetics. Use a voltage-mode PHY with on-chip MDI termination that permits each of the two center taps (CTs) to connect to GND through its own capacitor.

2. PHY-Side Connections

Connect MDI0± and MDI1± to T1A and T1B, respectively; do not add duplicate 49.9Ω termination to the data lines. CT_A and CT_B connect to GND through C1 and C2 (100nF each). Keep the CTs independent, without a bias supply, and place each capacitor close to its CT.

3. Magnetics and Cable Connections

T1 has two 1:1 isolation transformers with cable-side CMCs, forming a TD structure. Connect A± to RJ45 contacts 1/2 and B± to 3/6. The transmit/receive roles follow the PHY MDI/MDI-X configuration.

4. Bob Smith Termination and Shield

The two cable-side CTs connect to BS through R1 and R2. Join contacts 4/5 together and 7/8 together, then connect these groups through R3 and R4 to BS. R1-R4 are 75Ω each. BS connects through C3 (1nF, rated voltage ≥2kV) to SHIELD; the metal shell connects directly to the same SHIELD.

5. Implementation Scope

R1-R4 and C3 are external PCB components. Keep GND and SHIELD as separate nets and define their relationship at system level. Complete PHY power, clock, reset, MAC and LED circuits for the selected parts, and map functional names and cable-contact numbers to the actual package pins.

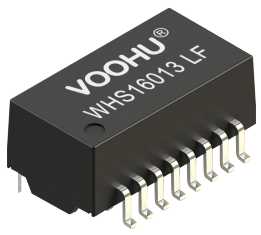
Product Illustrations



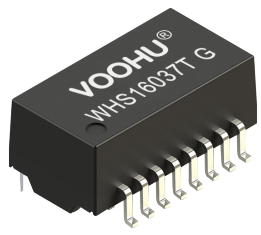
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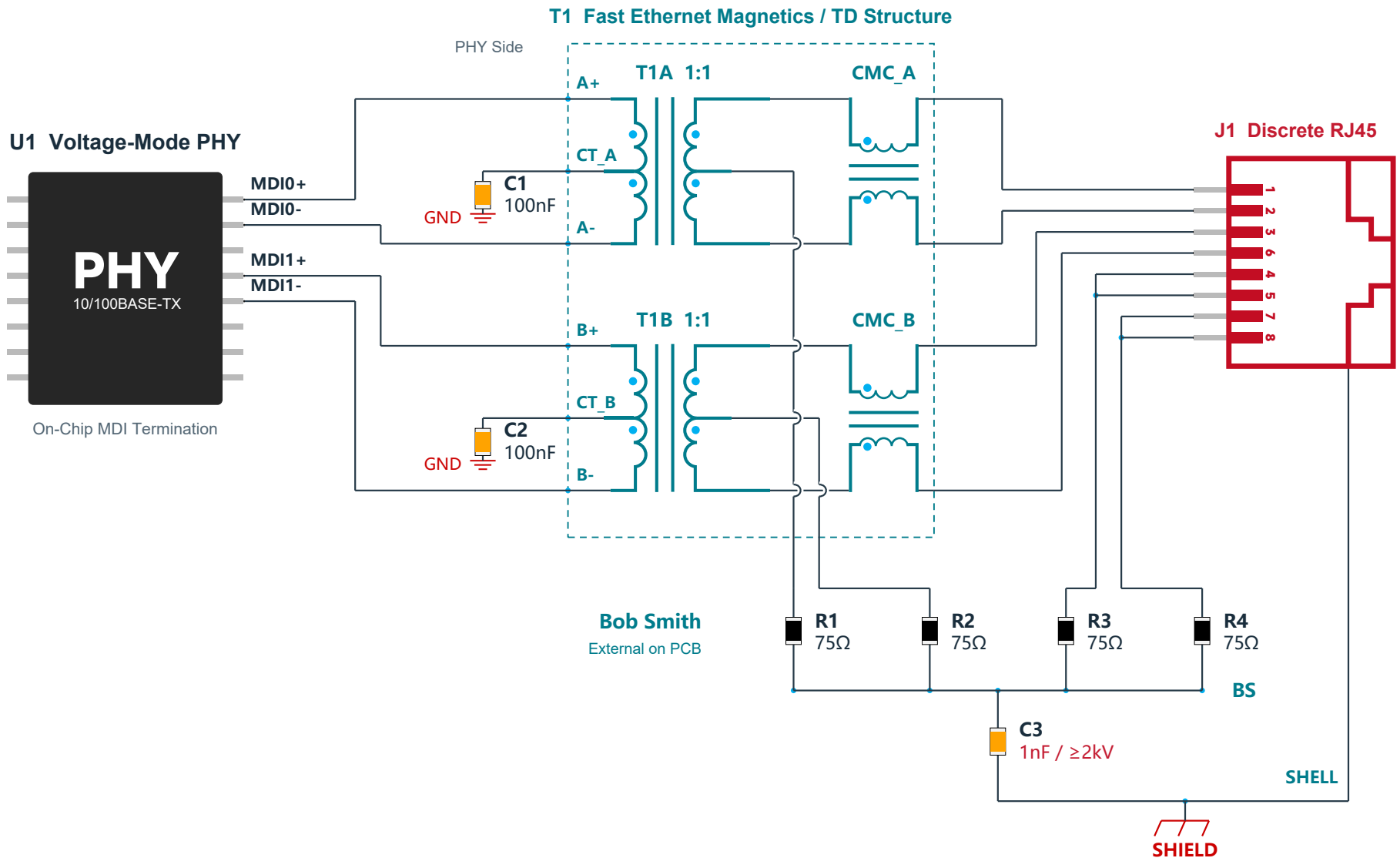


- WHS16013LF



- WHS16037TG (Industrial Grade)

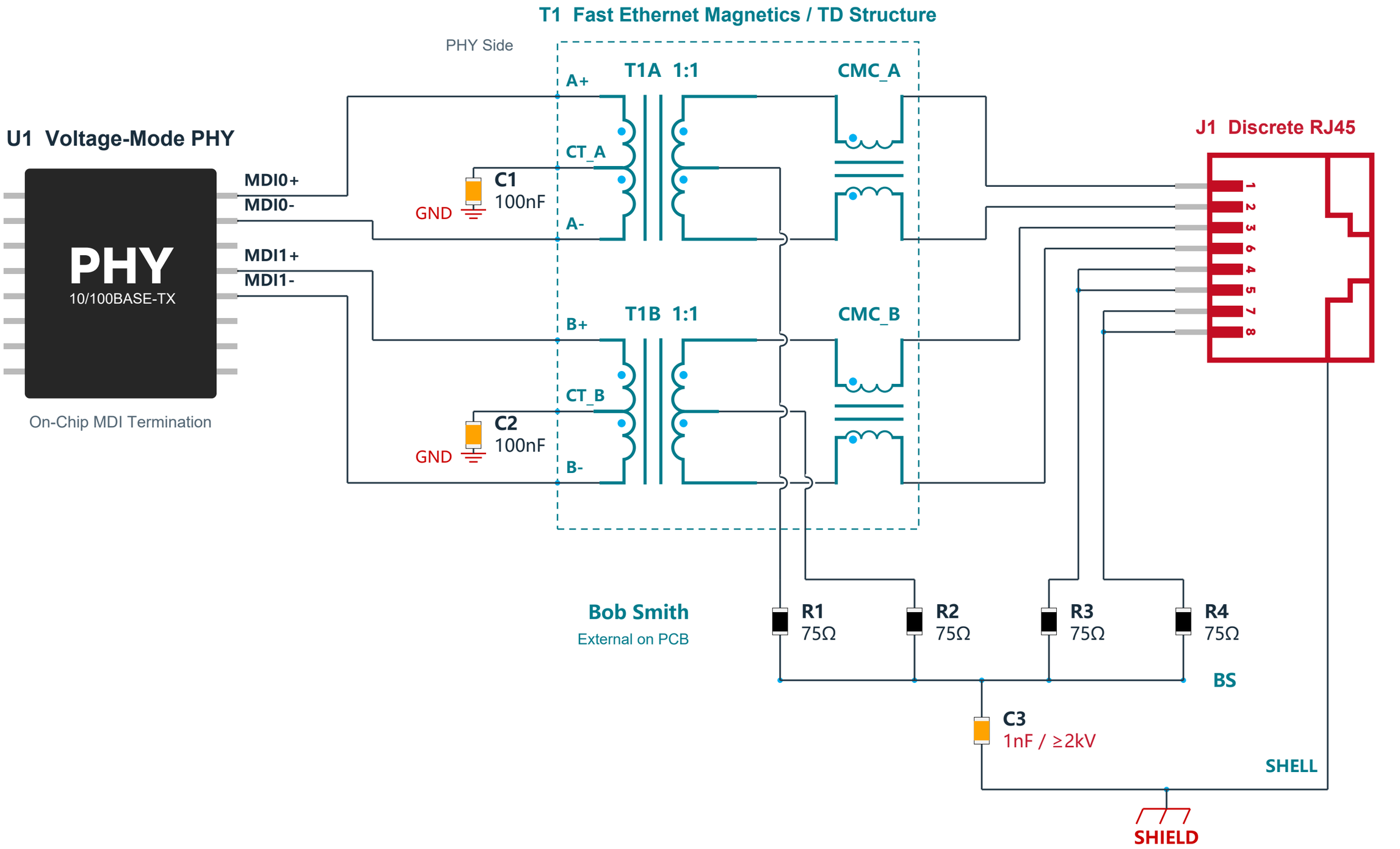
Reference Schematic



Reference circuit for design and component selection. Final connections, specifications and system performance depend on the selected parts and validation results.

10/100BASE-T Network Interface & Fast Ethernet Magnetics & Voltage-Mode PHY

Non-PoE | On-chip MDI termination | Each PHY-side CT connects to GND through 100nF



Functional names are not package pin numbers. RJ45 numbers identify cable contacts. Solid dot = connection; winding dot = polarity mark; wire jump = no connection.

Connections, Component Functions and Conditions of Use

Generic functional symbols are used in the schematic; the technical basis identifies specific Fast Ethernet devices and documents. This is an MDI interface reference, not a complete PHY design or a protection certification claim.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / Voltage-Mode PHY	1 device	Fast Ethernet architecture with on-chip MDI termination and capacitively grounded PHY-side CTs. No additional 49.9Ω termination or CT bias supply is fitted. The term "voltage-mode" alone does not determine all peripheral connections.	E1 p.42; E2 p.1
C1, C2 / 100nF	2, outside T1	Connect CT_A and CT_B individually to GND, providing an AC bypass for common-mode components while blocking DC. Keep the CTs independent, with one capacitor close to each pin. Select voltage rating, dielectric and package for the operating conditions.	Connection: E1 pp.42-43; CT proximity: E3 p.4
T1A, T1B / 1:1	2 channels, inside T1	Couple and isolate the two differential pairs. Both transformer sides have CTs. Magnetics must meet the selected PHY requirements for inductance, insertion loss, return loss, common-mode performance and insulation. The illustrated TD structure contains a transformer and CMC, with no autotransformer stage.	E1 pp.42-43, Table 28; E3 p.4, Fig.2
CMC_A, CMC_B	2 channels, inside T1	Two-winding common-mode chokes are in series with the cable-side data paths to attenuate common-mode interference. Keep the two windings and polarity marks paired; preserve separate differential paths and do not short the two data lines.	E1 p.42; E3 pp.4, 7
R1-R4 / 75Ω	4, outside T1	R1/R2 connect the two cable-side CTs to BS; R3/R4 connect the 4/5 and 7/8 groups. Each branch passes through 75Ω before joining BS. ±1% is an engineering selection recommendation. These are common-mode termination resistors, not PHY-side differential termination.	E3 p.4, Fig.2; p.6, §2.3; tolerance: engineering recommendation
C3 / 1nF, ≥2kV	1, outside T1	Connect BS through C3 to SHIELD for a high-frequency common-mode return with DC blocking. The voltage rating follows the manufacturer recommendation. Verify the selected part's AC/DC ratings, test conditions and insulation certification; its rating is not a system surge level.	E3 p.6, §2.3
J1 / Discrete RJ45	1 device	A± → 1/2; B± → 3/6. Contacts 4/5 form one group and 7/8 another; each group connects to BS through 75Ω. This applies only to this non-PoE Fast Ethernet use. Map cable-contact numbers to actual connector pins. Connect the metal shell to SHIELD.	E3 pp.4, 6-7; pair mapping per this schematic
GND / SHIELD	Two separate nets	GND returns the PHY-side capacitors; SHIELD connects the Bob Smith capacitor and metal shell. No fixed GND-to-SHIELD RC network is added. Define chassis/PE relationships and coupling locations from the enclosure, insulation and EMC design.	E3 p.7, §2.4; system coupling to be defined

Manufacturer Sources and Scope of Use (click to open)

E1 · Analog Devices

ADIN1200 Datasheet, Rev.B, May 2024. p.24, Table 18; pp.42-43, Magnetics, Fig.38 and Table 28; pp.86-87, PCB Layout. Used for MDI mapping, on-chip termination and independent 100nF connections to GND. Fig.38 contains an autotransformer stage; this design uses two-stage TD magnetics.

E2 · Texas Instruments

DP83825I Datasheet, SNLS638C, April 2026. p.1 and pp.86-87, §8.4: Fast Ethernet voltage-mode driver, on-chip MDI termination and 100Ω differential routing. Device-specific supply and package parameters are not transferred to the generic schematic.

E3 · Texas Instruments

AN-1469, SNLA079D, April 2013. p.4, Fig.2; p.6, §2.3; p.7, §2.4. Used only for isolated cable-side termination and shielding principles. The 1nF / ≥2kV recommendation is from the text on p.6; Fig.2 instead shows 1500pF. Its PHY-side supply and 49.9Ω termination are not adopted.

PCB Implementation and Component Selection

Route both MDI pairs for 100Ω differential impedance, keeping paths short and symmetric with minimal branches and layer changes. Maintain a continuous reference plane on the PHY side; determine copper clearances across the isolation region separately. Product images and model labels are retained for illustration only, without confirmed compatibility. After selecting the PHY, magnetics and RJ45, verify complete pin mapping, internal CT/CMC structure, 10M-mode specifications and magnetic parameters, then validate the link, return loss and EMC.

For component-selection review following document and schematic checks. No prototype testing, native EDA ERC or system certification testing has been performed.