Circuit Design

10GBASE-T Surge and ESD Protection & Current-Mode PHY

Design Overview

1. Structure and Conditions

Non-PoE; discrete shielded RJ45, external four-channel magnetics and reliable chassis/PE. Restricted to a PHY architecture with on-chip MDI termination, externally biased CTs and no CMS requirement. A compatible PHY and its parameters have not been established; this is an architecture revision draft.

2. Data Interface and CT Bias

A-D are four bidirectional MDI pairs mapped to RJ45 1/2, 3/6, 4/5 and 7/8. VCT_A-D identify separate CT bias nodes awaiting confirmation. C1-C4 provide local bypass to GND. Set voltages, capacitances and any shared CT supply connections from the selected PHY manufacturer's schematic.

3. Isolation and Common-Mode Termination

M1 contains four 1CT:1CT isolation transformers and cable-side two-line CMCs. Each cable-side CT connects through 75Ω to BS, then through CBS (1nF/HV*) to chassis. Arrange the four branches symmetrically. All eight contacts carry data.

4. Protection and Return Paths

D1-D4 connect across the PHY-side differential pairs. G1-G4 connect cable-side CTs to PE; coordinate high-voltage withstand and dynamic sparkover rather than assuming low-voltage GDTs. Connect the shell directly to the same PE and keep circuit GND separate. Bob Smith termination does not replace surge protection.

5. Targets and Implementation Limits

W1: CM ±4kV / DM ±2kV; E4: contact ±8kV / air ±15kV. P1/P2: 1500Vrms/60s. Surge and ESD both use R2 automatic recovery. These are test targets; PHY compatibility, protection selection and system results still require validation.

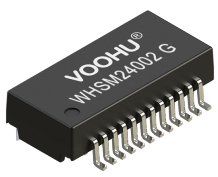
Product Illustrations



- SYT561188-AB1A3DY1027



- SYT60S1188-AB1A6DY1008



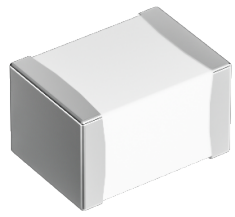
- WHSM24002G



- WHSM24P04P G

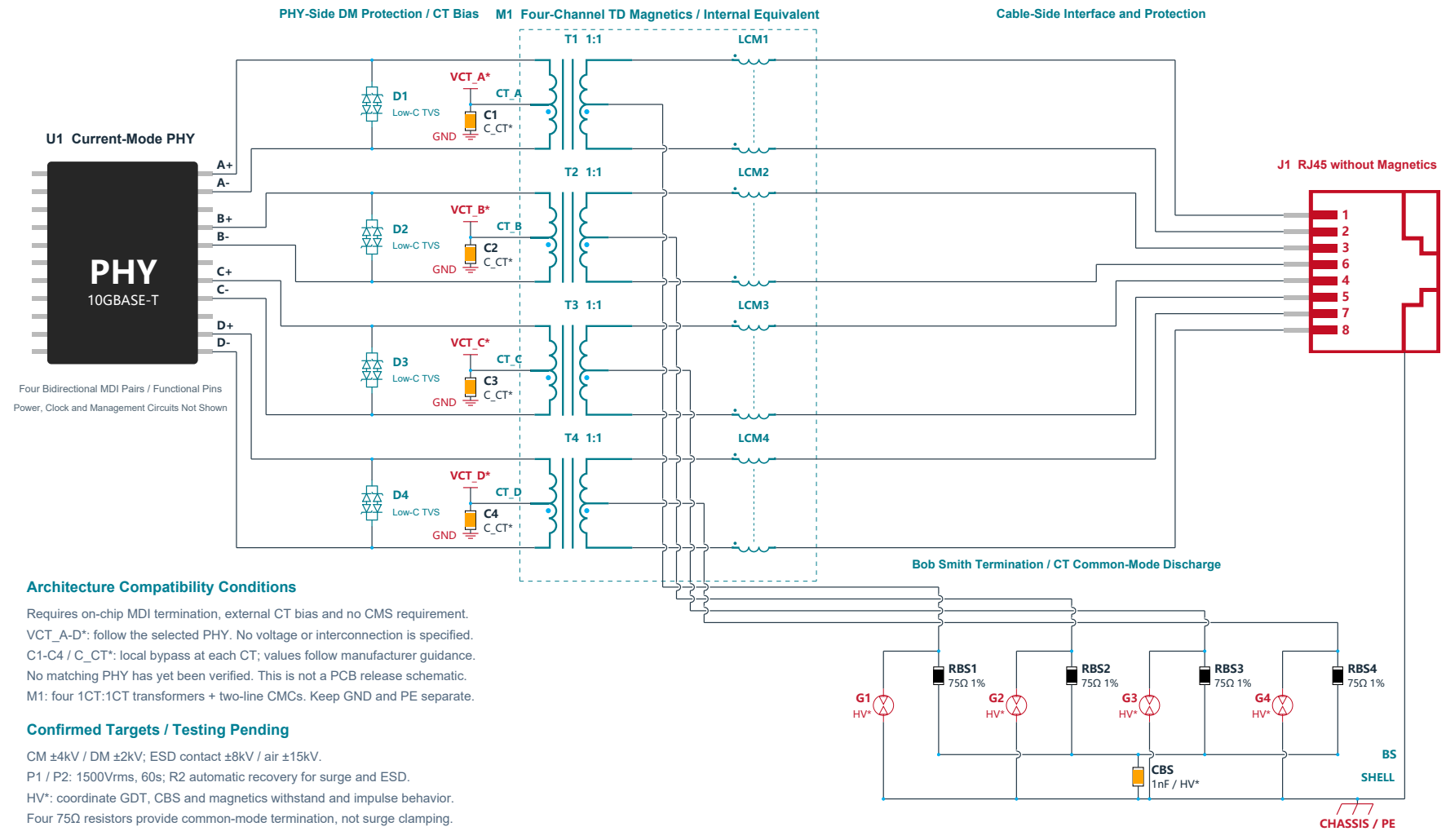


- WHTA5V01P2C



- WHGD200V1P0B

Reference Schematic



Architecture Compatibility Conditions

Requires on-chip MDI termination, external CT bias and no CMS requirement.
VCT_A-D*: follow the selected PHY. No voltage or interconnection is specified.
C1-C4 / C_CT*: local bypass at each CT; values follow manufacturer guidance.
No matching PHY has yet been verified. This is not a PCB release schematic.
M1: four 1CT:1CT transformers + two-line CMCs. Keep GND and PE separate.

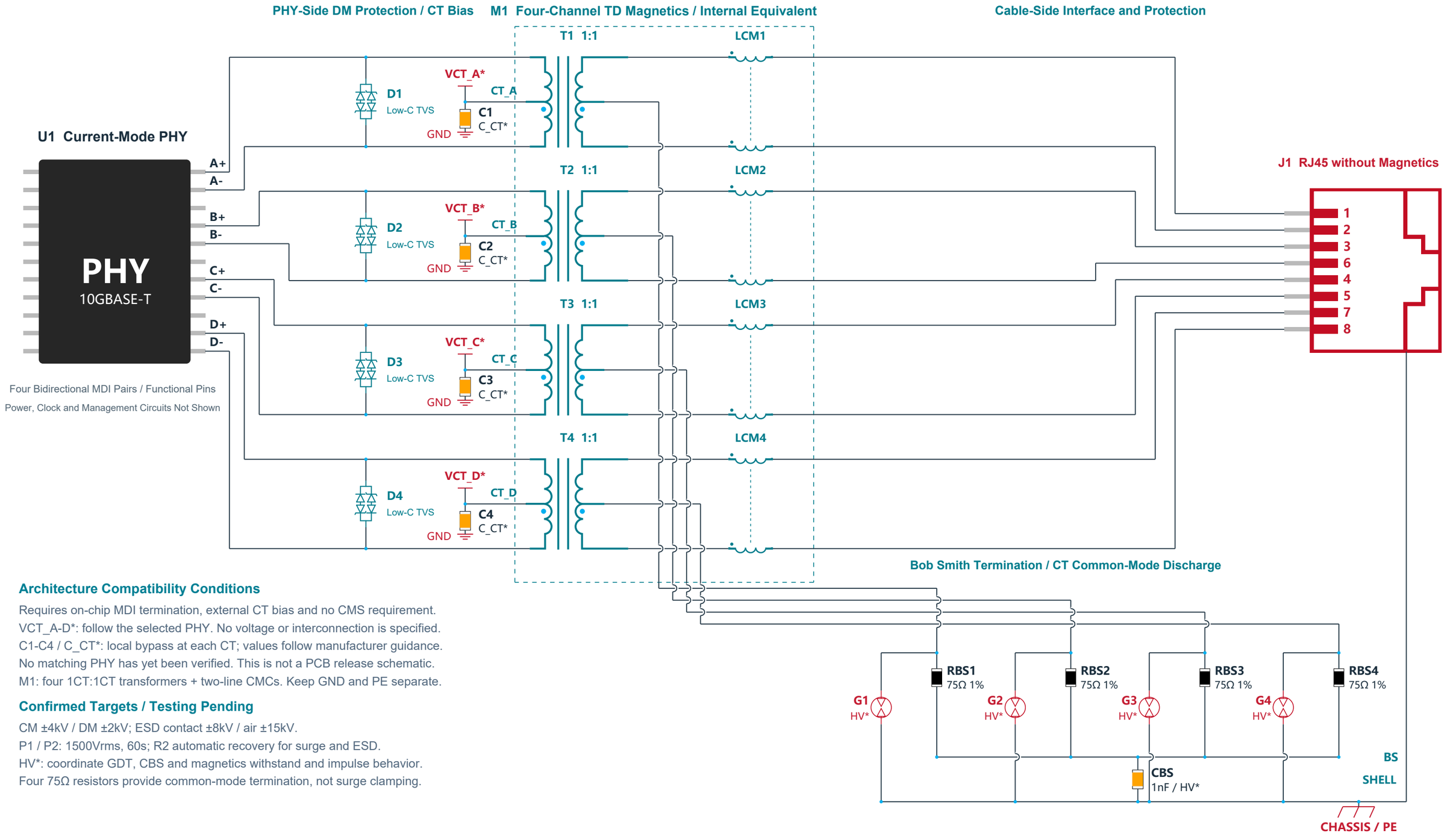
Confirmed Targets / Testing Pending

CM ±4kV / DM ±2kV; ESD contact ±8kV / air ±15kV.
P1 / P2: 1500Vrms, 60s; R2 automatic recovery for surge and ESD.
HV*: coordinate GDT, CBS and magnetics withstand and impulse behavior.
Four 75Ω resistors provide common-mode termination, not surge clamping.

Four-channel architecture revision draft. PHY bias/termination compatibility remains unresolved. Protection and 10G performance require validation; not ready for PCB fabrication.

10GBASE-T Surge and ESD Protection & Current-Mode PHY

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Functional names are not package pins. Dashed outline = M1 internal functions; same-name nodes connect. Solid dot = connection; wire jump = no connection; CMC dashed lines = magnetic coupling.

10G Interface Basis and Limits of the Added Protection

The four-channel magnetic structure was checked against a Bel drawing. Common-mode termination and protection methods follow Semtech and other original sources. The specific current-mode PHY, bias and termination evidence remain unresolved. This is a conditional architecture, not a reproduction of a validated reference board.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / VCT_A-D*	4 bidirectional pairs; bias pending	Assumes on-chip termination, externally supplied CTs and no CMS requirement. No specific PHY manufacturer schematic has been established that satisfies all these conditions. Do not infer VCT voltage/interconnections or external termination needs from the mode name. Not ready for PCB fabrication.	PHY evidence pending; [7][8] comparison only
M1 / T1-T4 / LCM1-LCM4	4 × 1CT:1CT; 4 × two-line CMC	Only four data magnetic channels remain. CMCs are on the cable side; CTs are brought out independently. Internal functional designators do not imply eight external BOM components. Match the assembly to the actual PHY and 10G link.	[1]; compatibility unverified
C1-C4 / C_CT*	4 local CT bypasses; values pending	Each connects its own VCT to circuit GND locally. Do not assume a common supply, 2.5V or 4.7µF. After selecting the PHY, determine capacitance, rating, effective capacitance and supply decoupling.	PHY manufacturer schematic pending
RBS1-RBS4 / CBS	4 × 75Ω 1%; 1nF / HV*	Four cable-side CTs pass through 75Ω to BS. CBS blocks DC and returns common-mode current to chassis. The 1% tolerance is an engineering selection. Verify pulse energy, CBS AC/impulse capability and parasitics. A 1nF value does not establish a protection level.	[2]; tolerance / HV*: engineering qualification
D1-D4	4 × low-C bidirectional TVS; PHY-side across-pair	Limit differential stress transferred to the PHY side. Working voltage must cover the signal and residual voltage must stay within PHY transient limits. Check parasitics and energy. A manufacturer 500V example cannot establish a pass at the 2kV differential target.	[2]; parts not selected
G1-G4 / HV*	4 high-voltage GDTs; cable CT to PE	Must withstand P2 with all parts fitted without firing; verify maximum dynamic sparkover. A high-voltage GDT may not fire at or below 4kV. Magnetics, CBS and clearances cannot rely on guaranteed firing; validate the 5kV engineering margin.	[3][4]; engineering extension
J1 / GND / PE	Shielded RJ45 without magnetics; non-PoE	Keep 1/2, 3/6, 4/5 and 7/8 as four intact differential pairs. Connect the shell directly to reliable chassis/PE. Circuit GND is separate; do not connect cable-side CT return paths or protection parts to PHY-side GND.	[1][2]; system grounding design

Test Conditions and Acceptance Targets

Surge W1 / R2	CM ±4kV: all eight lines, 40Ω coupling + 2Ω source. DM ±2kV: additional project-specific, floating 42Ω loop applied to each pair.
Coupling / Waveforms	Calibrate CM per IEC Table 10; nominal total Isc is 96A at 4kV. Verify 10G transparency separately. The generator's 8/20µs waveform is not the CDN output waveform.
ESD E4 / R2	Contact ±8kV; air ±15kV, including applicable accessible points and indirect discharge. Test points and counts are defined in the full protocol.
P1 / P2 / R2	P1 and P2: 1500Vrms, 50/60Hz, 60s, with protection parts fitted. Engineering limit: automatically restore 10G within 60s; no manual reset.

Manufacturer Sources and Scope of Use (click to open)

[1] · Bel	S558-10GB-05, electrical drawing Rev.E, June 29, 2020; downloaded PDF p.1.
[2] · Semtech	Ethernet Protection Methodology, February 19, 2020, Figs.1 and 4.
[3] · Littelfuse	General Port Protection Spotlight, 2024, pp.8 and 10.
[4] · Bourns	GDT28H, p.1: AC withstand, impulse sparkover voltage and surge ratings.
[5] · IEC	61000-4-5:2014+A1:2017; 2014 text §6.3.3.3 and Tables 9/10 checked.
[6] · IEC	61000-4-2:2025: system-level contact, air and indirect discharge methods.
[7] · Intel	X540 Datasheet v3.1, §§13.2.2-13.2.4 and §13.2.8; used only to identify an excluded architecture.
[8] · Intel	X550 Datasheet Rev.2.7, §13.2.7, p.1148; used only to identify an excluded architecture.

Validation Scope

Status: four-channel architecture revision draft with unresolved PHY evidence. Text, connectivity and visual assets have been checked; native EDA ERC and physical testing have not been performed. Obtain a specific PHY manufacturer schematic to resolve VCT*, C_CT* and termination compatibility before PCB release. Confirmed protection targets remain unchanged. Cat6A U/UTP is the test baseline; the 5kV margin and 60s recovery limit are engineering agreements. Full procedures, entry criteria and open items are in records 09/11 of the Chinese design package.

Schematic text and connection data have been checked; no native EDA ERC or physical testing has been performed. Original product images and model labels are retained only for illustration, without a compatibility claim.