Circuit Design

D1.0

10GBASE-T Surge and ESD Protection & Voltage-Mode PHY

Non-PoE | Discrete RJ45 + external 10G magnetics | TVS across each differential pair

Design Overview

1. PHY and Center Taps

Use a 10G voltage-mode PHY with on-chip termination and four bidirectional MDI pairs. CT_A-CT_D connect individually through C1-C4 (100nF each) to GND. Keep each capacitor close to its magnetics pin. Do not apply an external CT bias supply.

2. Magnetics and Pair Mapping

T1 contains four 1:1 isolation transformers with cable-side CMCs (TD structure) and must meet the selected PHY's 10G magnetics requirements. Map A/B/C/D to RJ45 contacts 1/2, 3/6, 4/5 and 7/8. All four are data pairs.

3. Surge and ESD Clamping

D1-D4 are low-capacitance bidirectional TVS devices, one across the positive and negative lines of each MDI pair. Place them close to the PHY side of the magnetics with short connections to limit coupled differential transients. Match working voltage, clamping behavior and parasitic capacitance to the actual PHY.

4. Common-Mode Termination and Shield

Each cable-side CT connects through R1-R4 (75Ω each) to BS, then through C5 (1nF high-voltage capacitor) to SHIELD. The RJ45 shell shares SHIELD. Bob Smith termination provides common-mode termination, not TVS clamping.

5. Scope

Non-PoE; for on-chip termination and capacitively grounded CTs. GND and SHIELD are separate. This is a port-protection reference for induced surges and ESD; target levels and chassis-grounding conditions remain to be defined. Complete the other circuitry for the selected PHY.

Product Illustrations



- SYT561188-AB1A3DY1027



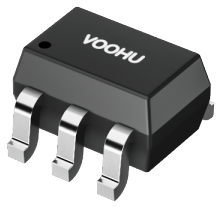
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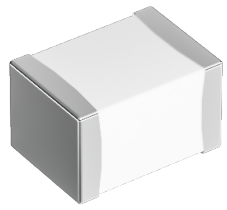
- WHSM24002G



- WHSM24P04P G

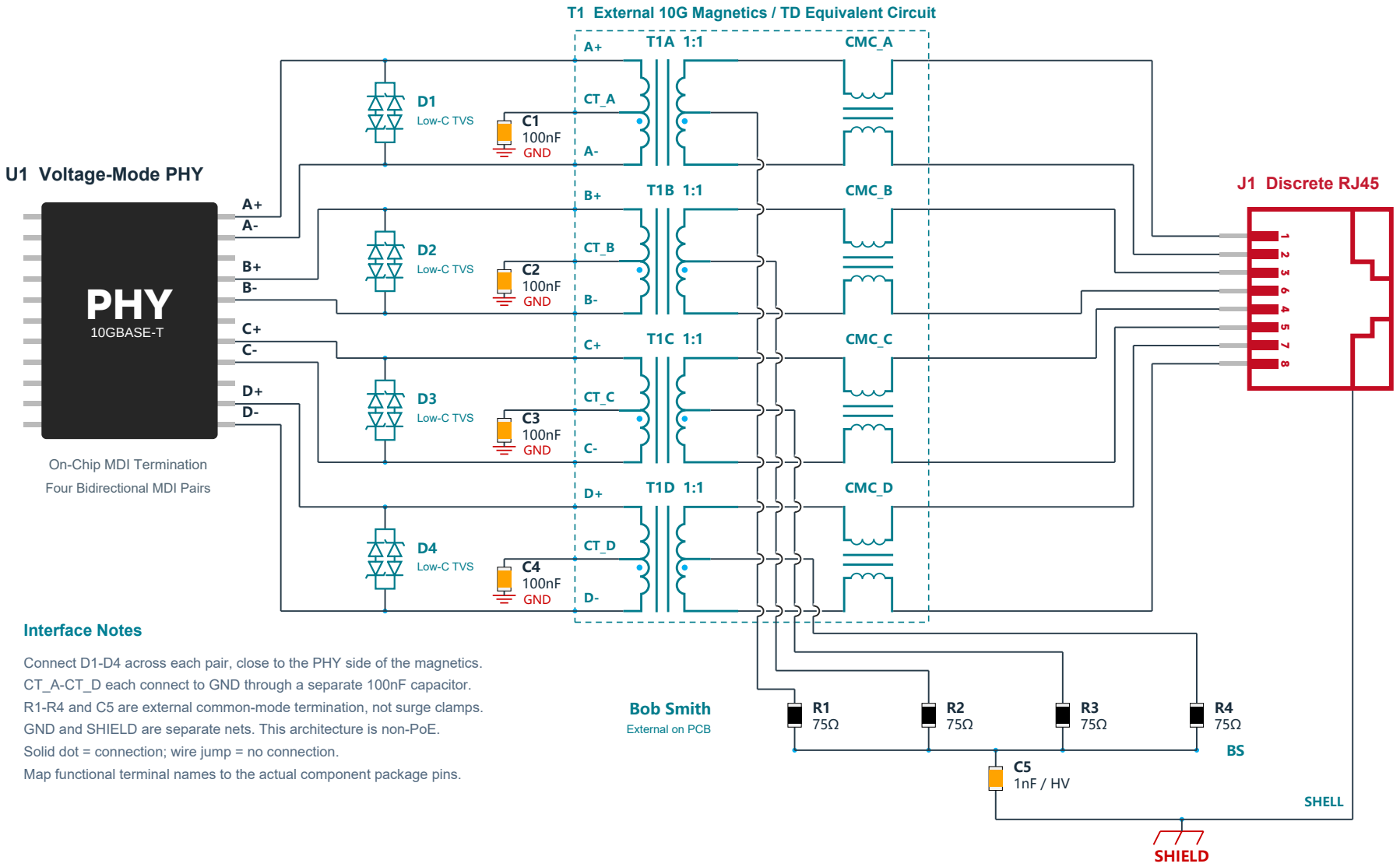


- WHTA5V01P2C



- WHGD200V1P0B

Reference Schematic

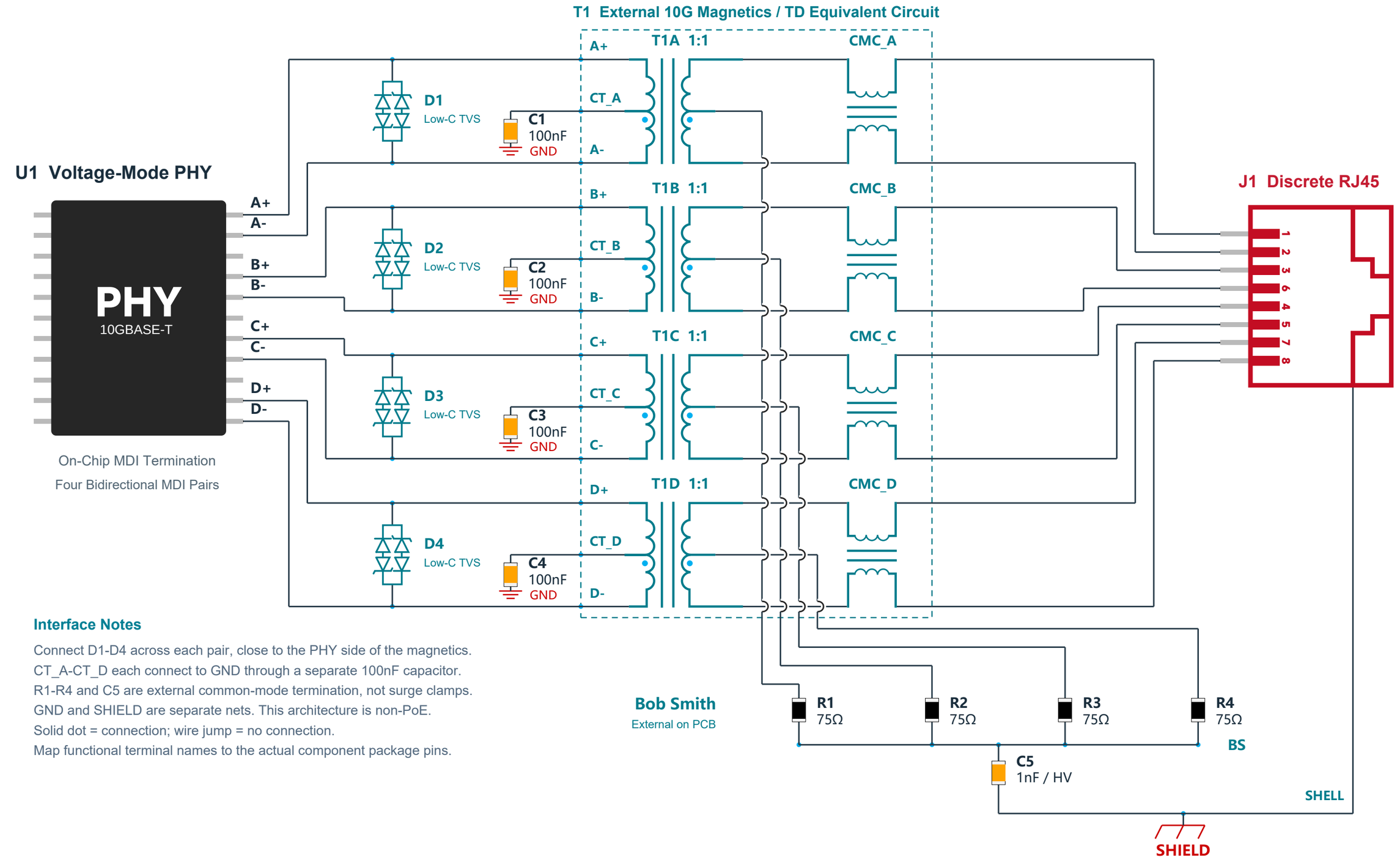


Interface Notes

Connect D1-D4 across each pair, close to the PHY side of the magnetics.
CT_A-CT_D each connect to GND through a separate 100nF capacitor.
R1-R4 and C5 are external common-mode termination, not surge clamps.
GND and SHIELD are separate nets. This architecture is non-PoE.
Solid dot = connection; wire jump = no connection.
Map functional terminal names to the actual component package pins.

10GBASE-T Surge and ESD Protection & Voltage-Mode PHY

Non-PoE | Voltage-mode PHY with on-chip termination | Line-to-line clamping on the PHY side of the magnetics



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10G Design Sources and Component Coordination

The following defines the sources used for this independent design. Components are shown generically; manufacturer part numbers identify sources, not mandatory purchases or system compliance.

Component / Value	Qty / Location	Design Rationale and Constraints	Source
U1 / Voltage-Mode PHY	1 device	Use a 10G architecture with on-chip MDI termination and CTs requiring capacitive decoupling only. Do not duplicate termination with external 49.9Ω resistors or a 100Ω differential resistor. Complete power, clock, reset, management and MAC interfaces for the actual PHY.	E1 pp.59-60,91; E2 schematic p.12
C1-C4 / 100nF	4, outside T1	Connect each PHY-side CT individually to GND to provide an AC common-mode return. Place capacitors locally. Do not short the CTs together or connect them to an external supply. 100nF is the reference architecture value, taken directly from a manufacturer's 10G circuit.	E2 p.12: C501, C502, C504, C505
D1-D4 / Low-C Bidirectional TVS	4, PHY side	Connect one bidirectional clamp across the positive and negative lines of each pair. The symbol represents a two-terminal clamping function only. Working voltage must cover normal line-to-line swing and the clamp waveform must remain within PHY transient tolerance. Verify capacitance, residual voltage and pulse capability for this line-to-line connection.	E3 Fig.4; E4 10G applications
T1A-T1D / 1:1	4 channels, inside T1	Transfer differential signals through magnetic coupling and provide galvanic isolation. Select 10G magnetics meeting the PHY requirements for insertion loss, return loss, crosstalk, balance, OCL and insulation. An identical turns ratio alone does not establish compatibility.	E1 pp.59-60; E2 p.12; E3
CMC_A-CMC_D	4 channels, inside T1	Two-winding CMCs in series with both cable-side data lines suppress common-mode interference. They form TD channels with the isolation transformers; no autotransformer winding is included. Include magnetics and package parasitics in the 10G signal-integrity assessment.	E3 Figs.1,4; verify selected magnetics
R1-R4 / 75Ω	4, external on PCB	Each cable-side CT connects through its own 75Ω resistor before joining BS. These resistors are not in series with the main differential path. Verify pulse loading and voltage withstand; steady-state power rating alone does not establish surge capability.	E3 Figs.1,2
C5 / 1nF, HV	1, external on PCB	The high-voltage capacitor connects BS to SHIELD, providing an AC common-mode return and blocking DC. HV requires a part selected for the actual insulation and pulse tests. Rated DC voltage, AC withstand voltage and surge immunity level are not interchangeable.	E3 Figs.1,2
J1 / GND / SHIELD	Discrete RJ45; separate ground nets	Map A to 1/2, B to 3/6, C to 4/5 and D to 7/8. The RJ45 has no magnetics. Its shell and the return side of C5 connect to SHIELD; C1-C4 connect to GND. Chassis bonding of SHIELD and any PE connection depend on the complete system.	E1 pp.59-60; E3 Figs.1,4

Technical Sources and Scope of Use

E1 · Aquantia / Marvell — AQR113/C family datasheet, Rev.1.0.7 (October 2018), pp.59-60 and §4.13, p.91: 10G MDI, 1:1 magnetics and voltage-mode CT decoupling. The linked file is a public reproduction of manufacturer-attributed material; obtain the applicable version for production.

E2 · NXP — LS1046ARDB-PB, SPF-29142 Rev.C, p.12: all four AQR113C CTs connect individually to GND through 0.1µF, without external MDI termination. Only the PHY-side connection is used; the board's CMS and special connector internal network are not adopted.

E3 · Semtech — Ethernet Protection Methodology (2020-02-19), Figs.1-4: PHY-side line-to-line clamping, common-mode termination and protection coordination. Its 500V, 1.2/50µs, 42Ω example results do not prove compliance of this circuit or a higher test level.

E4 · Semtech — Official RClamp3361P documentation lists 2.5G/5G/10GbE applications: ±3.3V working voltage, 0.2pF typical capacitance and 7A peak current at 8/20µs. These are selection references only. A component rating is not a port immunity rating.

PCB Implementation and Validation

Route MDI pairs for a 100Ω differential target. Minimize TVS stubs, control within-pair skew and assess discontinuities from pads, vias and magnetics. Validate 10G links, return/insertion loss, EMC and insulation. IEC 61000-4-5 / -4-2 tests must define waveform, source impedance, coupling method, common/differential mode, polarity, test count and pass criteria.

To be defined: surge/ESD targets and chassis/PE conditions. This reference uses transformer isolation plus line-to-line TVS protection and contains no GDT. Higher-energy protection requires further coordination. Product images are retained as illustrations; confirm 10G and protection compatibility from the actual component documentation.